



abit M703 IX38 MAX Schematics

Version: 0.2

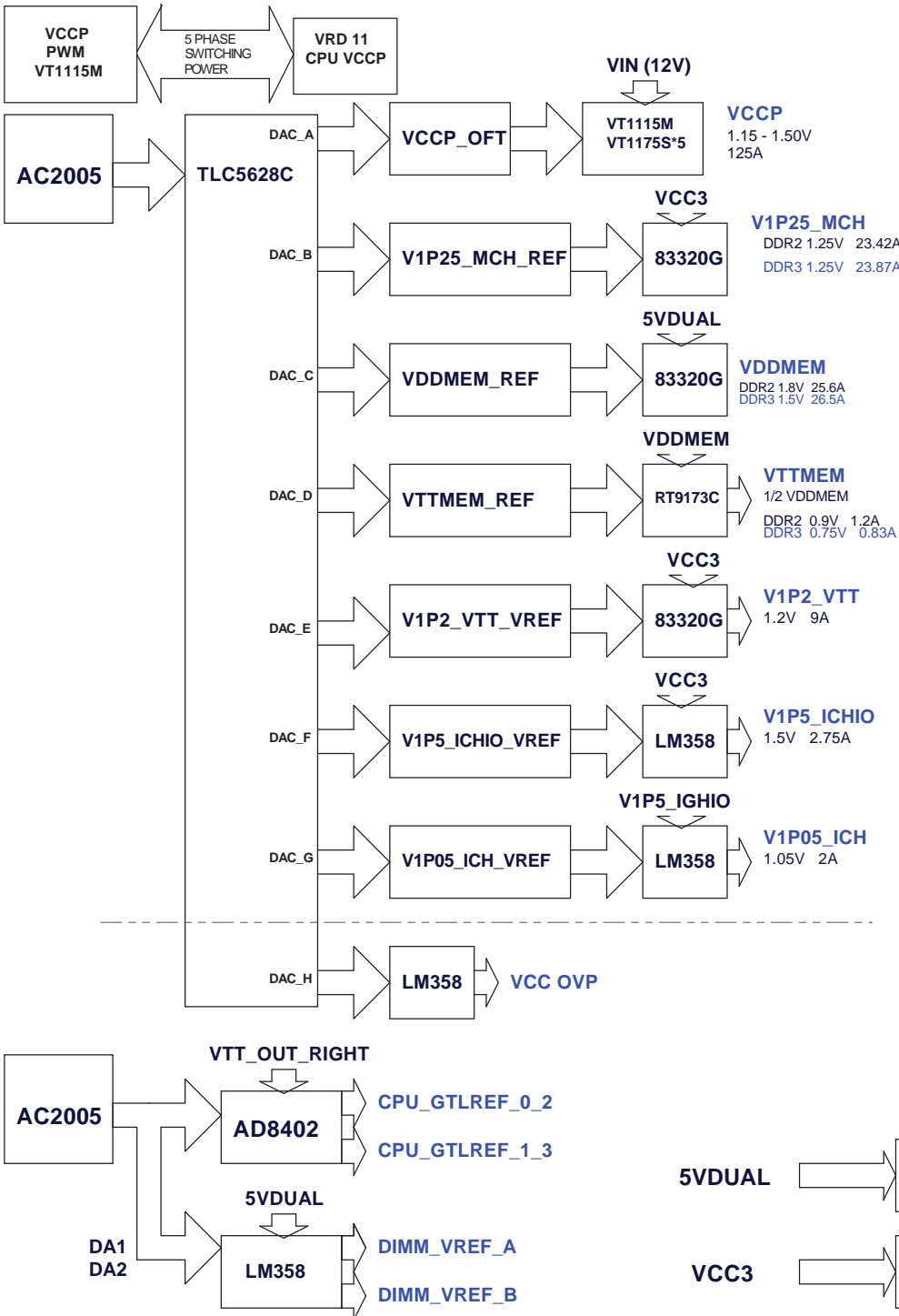
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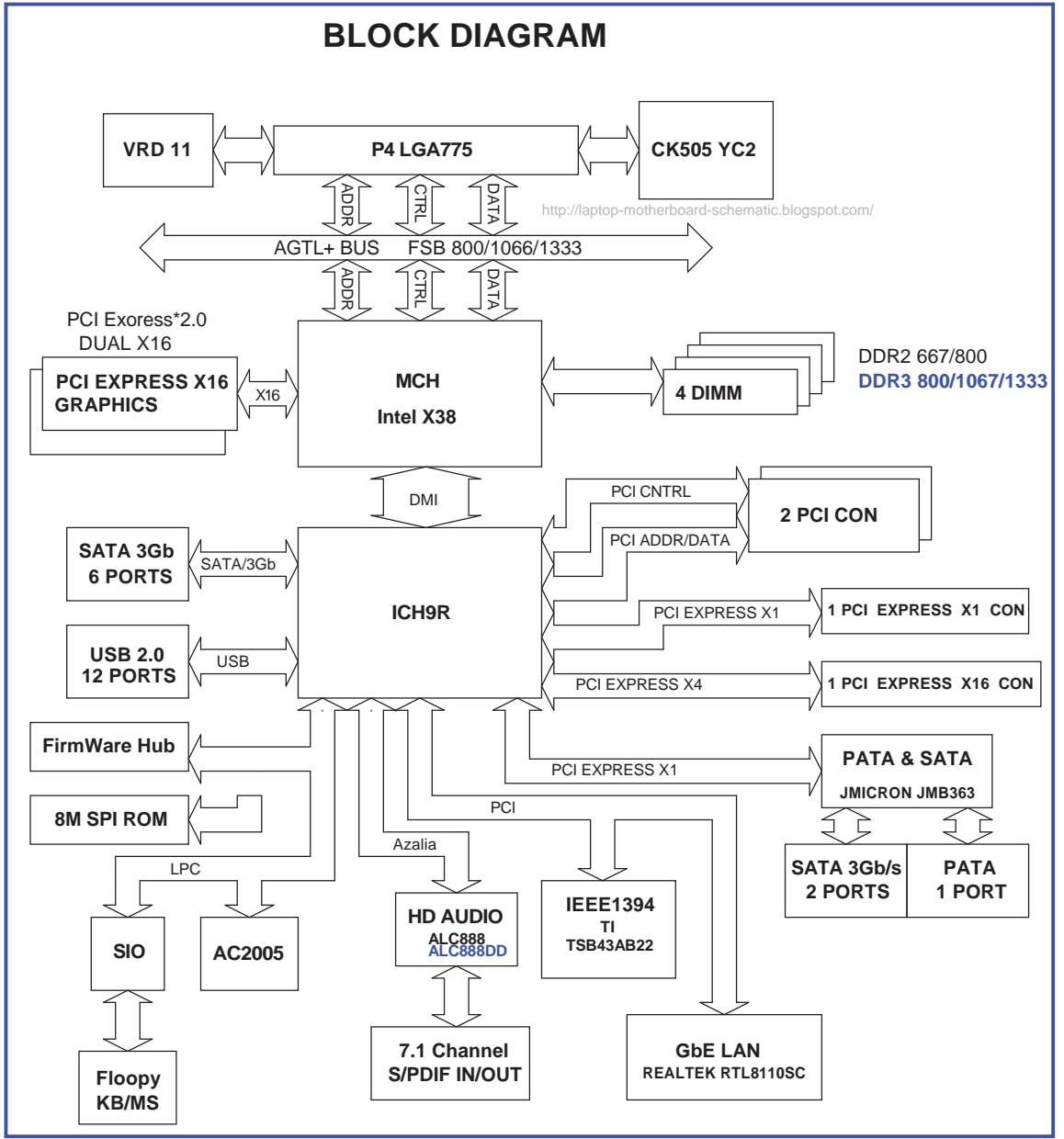
Model	SSID	PCB	Features
IX38 MAX	108A	Black	uGuru Tech., Silent OTES 2, Dual DDR3 1333/1066 Dual SATA 3Gb/s RAID, eSATA, PATA, GbE IEEE-1394, 7.1 Channel HD Audio Back LED
IX38 QuadGT	108B	Blue	uGuru Tech., Silent OTES 2, Dual DDR2 800, Dual SATA 3Gb/s RAID, eSATA, PATA, GbE IEEE-1394, 7.1 Channel HD Audio

 	
COVER SHEET	
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POWER DESIGN DIAGRAM



BLOCK DIAGRAM



ICH9 GPIO SETTING


Pin Name	Power Well	Usage	Default
GPIO0	3.3V Core	ACZ_DET	GPI
GPIO1	3.3V Core	TACH1	GPI
GPIO2	5V Core	PIRQ#E	GPI
GPIO3	5V Core	PIRQ#F	GPI
GPIO4	5V Core	PIRQ#G	GPI
GPIO5	5V Core	PIRQ#H	GPI
GPIO6	3.3V Core	TACH2	GPI
GPIO7	3.3V Core	TACH3	GPI
GPIO8	3.3V Sus	LPC_PME#	GPI
GPIO9	3.3V Sus	WOL_EN	Native
GPIO10	3.3V Sus	GPIO10	GPI
GPIO11	3.3V Sus	SMBALERT#	Native
GPIO12	3.3V Sus	LAN_PME#	GPI
GPIO13	3.3V Sus	1394_PME#	GPI
GPIO14	3.3V Sus	LAN2_PME#	GPI
GPIO15	3.3V Sus	STP_PCI#	Native
GPIO16	3.3V Core	FWH_WP#	GPO
GPIO17	3.3V Core	TACH0	GPI
GPIO18	3.3V Core	GPIO18	GPO
GPIO19	3.3V Core	SATA1GP	GPI
GPIO20	3.3V Core	GPIO20	GPO
GPIO21	3.3V Core	SATA0GP	GPI
GPIO22	3.3V Core	SCLOCK	Native
GPIO23	3.3V Core	LDRQ1#	Native
GPIO24	3.3V Sus	CLGPIO0	GPO
GPIO25	3.3V Sus	STP_CPU#	Native
GPIO26	3.3V Sus	S4_STATE#	GPO
GPIO27	3.3V Sus	EL_STATE0	GPO
GPIO28	3.3V Sus	EL_STATE1	GPO
GPIO29	3.3V Sus	OC5#	Native
GPIO30	3.3V Sus	OC6#	Native
GPIO31	3.3V Sus	OC7#	Native
GPIO33	3.3V Core	BORAD ID	GPO
GPIO34	3.3V Core	BOARD ID	GPO
GPIO35	3.3V Core	SATACLKREQ#	GPO
GPIO36	3.3V Core	SATA2GP	GPI
GPIO37	3.3V Core	SATA3GP	GPI
GPIO38	3.3V Core	SLOAD	GPI
GPIO39	3.3V Core	SDATAOUT0	GPI
GPIO40	3.3V Sus	OC1#	Native
GPIO41	3.3V Sus	OC2#	Native
GPIO42	3.3V Sus	OC3#	Native
GPIO43	3.3V Sus	OC4#	Native
GPIO44	3.3V Sus	OC5#	Native
GPIO45	3.3V Sus	OC6#	Native
GPIO46	3.3V Sus	OC7#	Native
GPIO47	3.3V Sus	OC8#	Native
GPIO48	3.3V Core	SDATAOUT0	GPI
GPIO49	V_CPU_IO	CPUPWRGD	Native
GPIO50	5.5V Core	REQ1#	Native
GPIO51	3.3V Core	GNT1#	Native
GPIO52	5.5V Core	REQ2#	Native
GPIO53	3.3V Core	GNT2#	Native
GPIO54	5.5V Core	REQ3#	Native
GPIO55	3.3V Core	GNT3#	Native

ICH9 GPIO SETTING

Pin Name	Power Well	Usage	Default
GPIO56	3.3V Sus	EXP_PRSNT1	GPI
GPIO57	3.3V Sus	EXP_PRSNT2	GPI

PCI DEVICE SETTING

DEVICE	PCI1	PCI2	1394	GbE
INTA	G	E	F	H
INTB	H	F		
INTC	E	G		
INTD	F	H		
IDSEL	18	19	17	16
REQ/GNT	2	3	1	0



GPIO SETTING

Size

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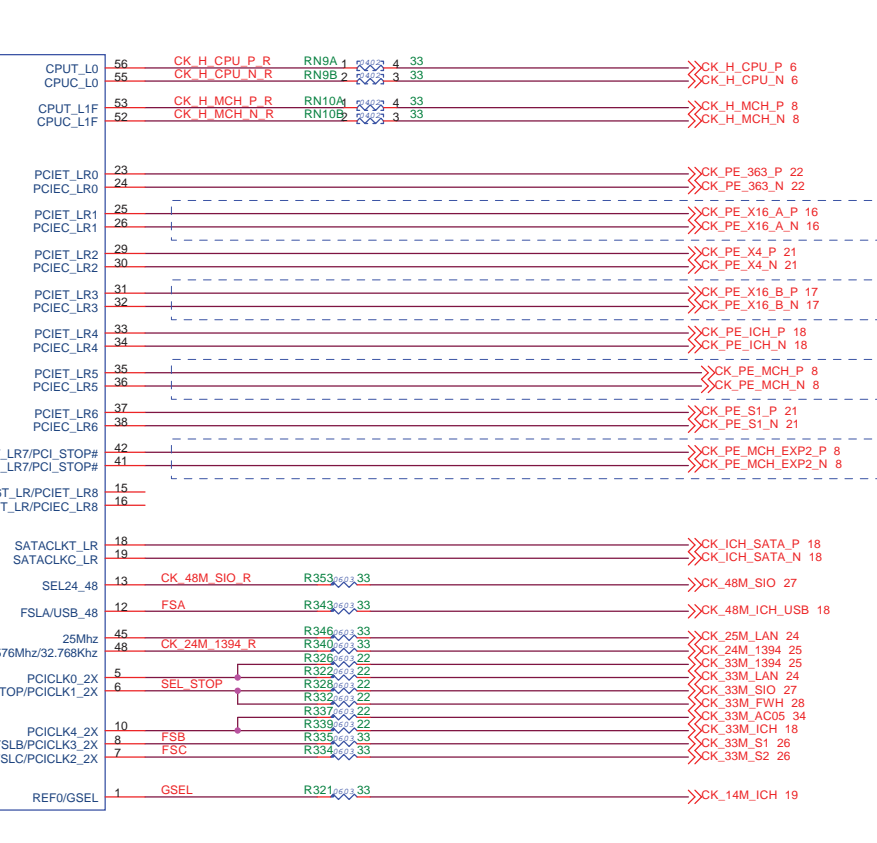
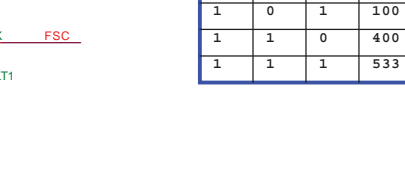
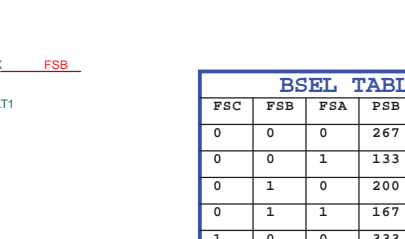
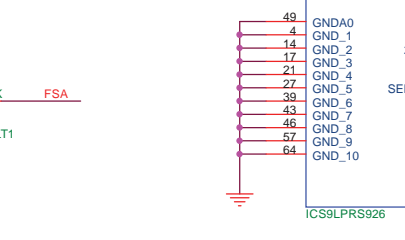
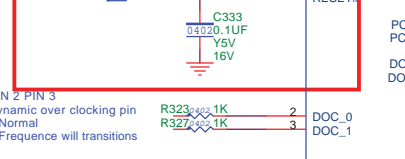
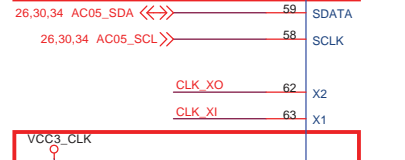
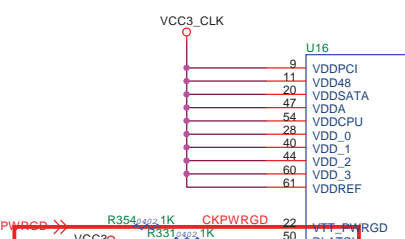
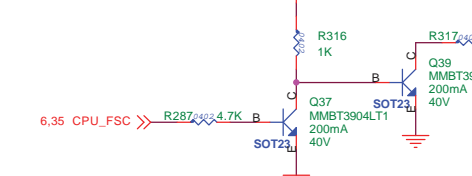
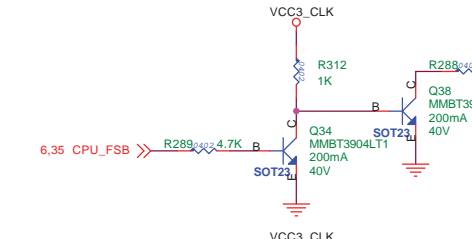
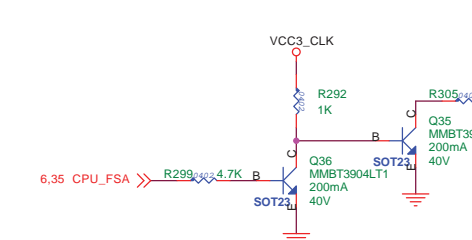
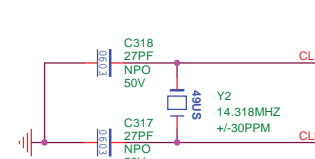
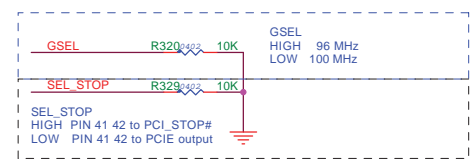
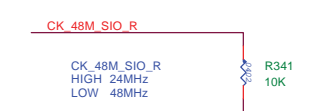
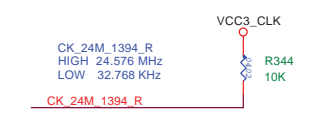
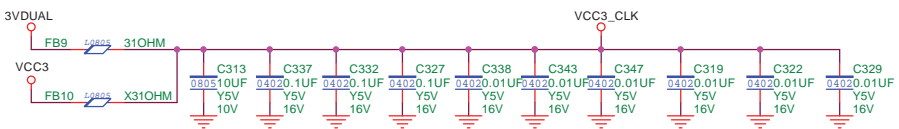
Custom

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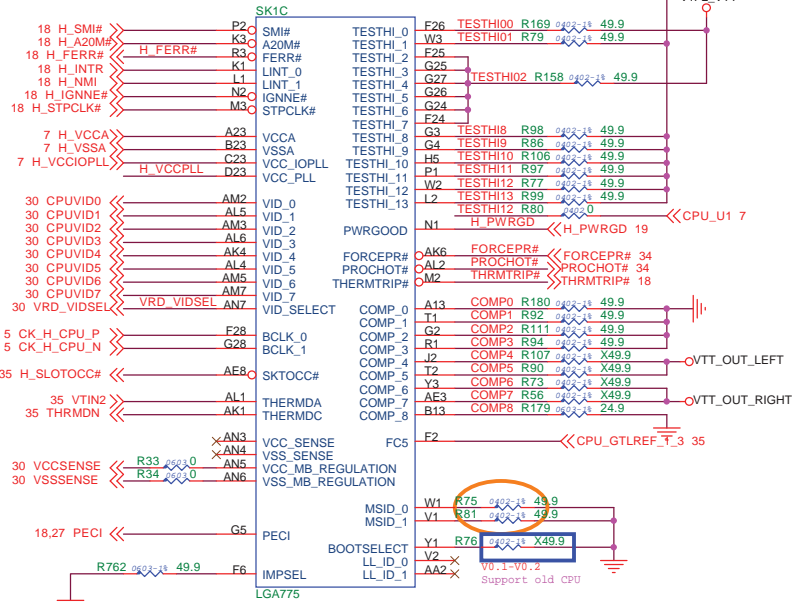
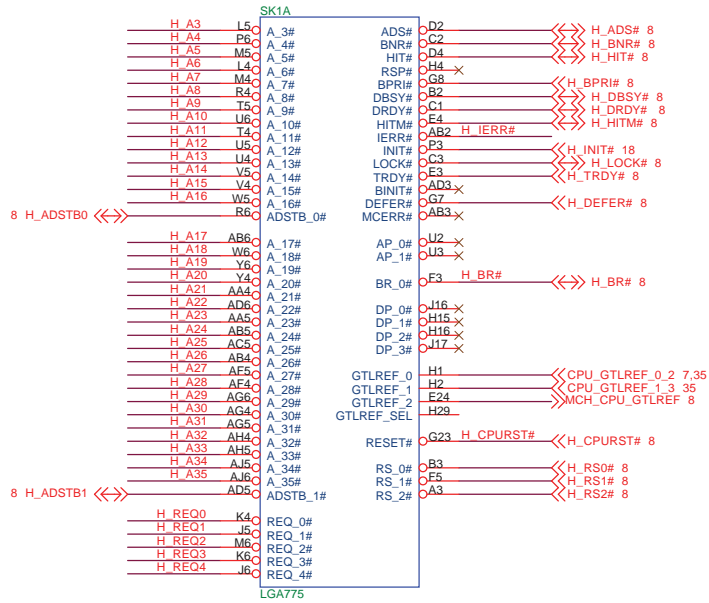
Support intel CK505 SPEC. GEN 2
SRC (1, 3, 5, 7) 4pairs Ops delay skew

BSEL TABLE			
FSC	FSB	FSA	FSB FREQUENCY
0	0	0	267 MHZ (1067)
0	0	1	133 MHZ (533)
0	1	0	200 MHZ (800)
0	1	1	167 MHZ (133)
1	0	0	333 MHZ (1333)
1	0	1	100 MHZ (133)
1	1	0	400 MHZ (RSVD)
1	1	1	533 MHZ (133)

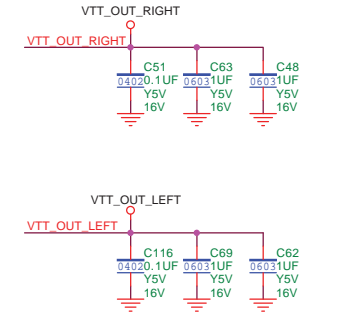
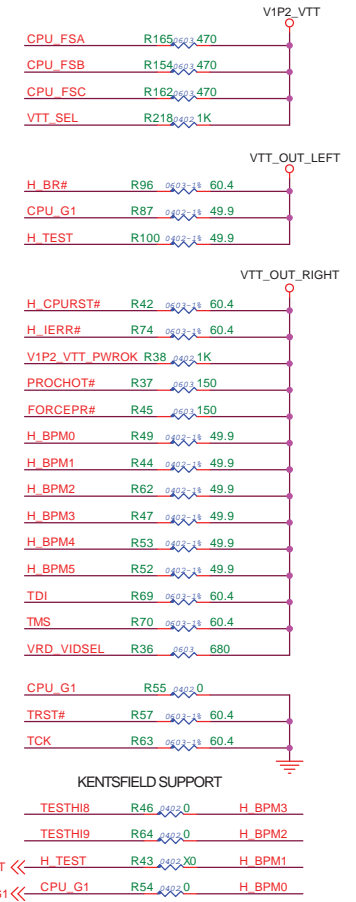
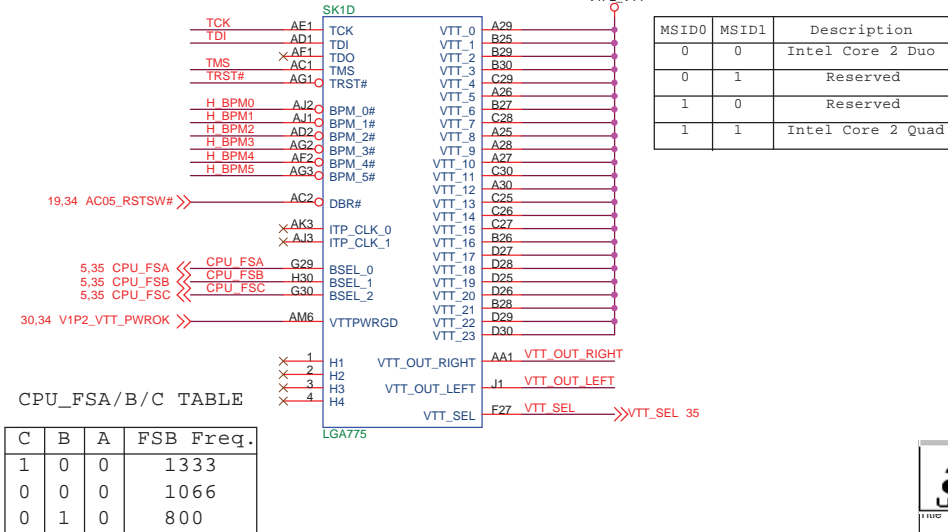
CLOCK SYNTHESIZER

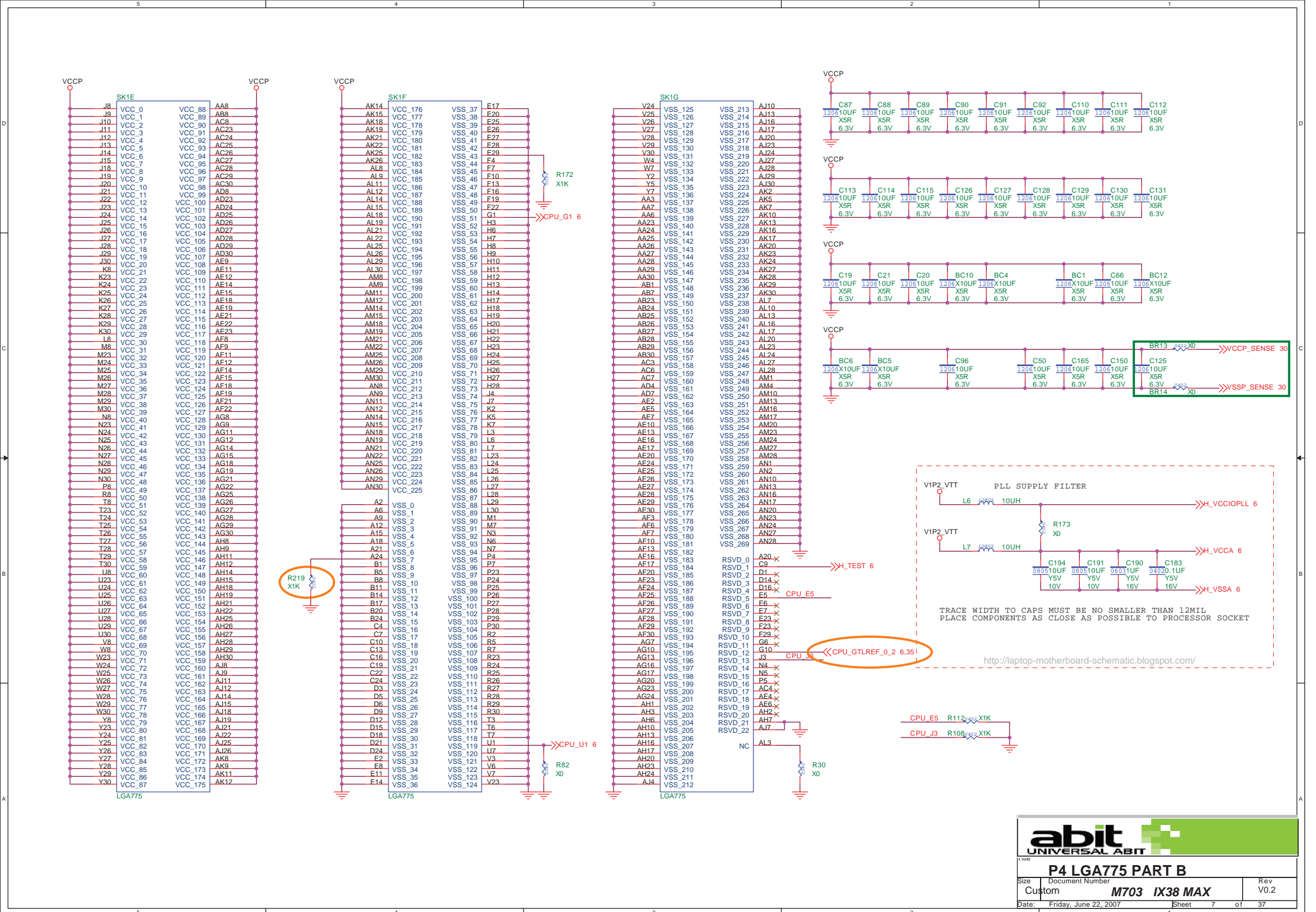
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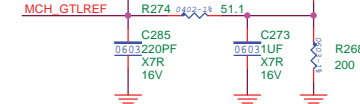
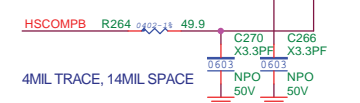
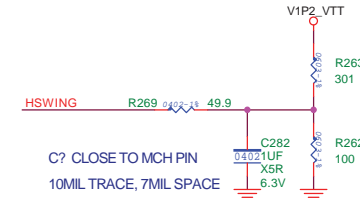
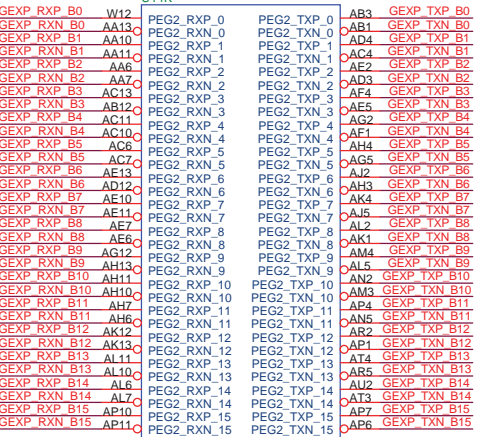
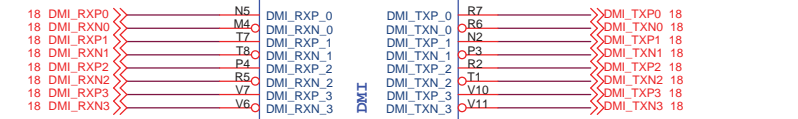
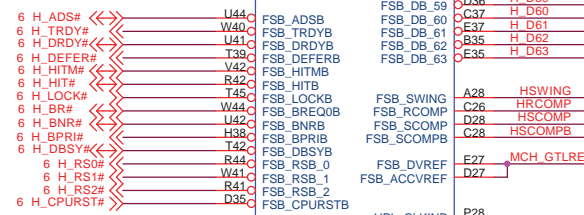
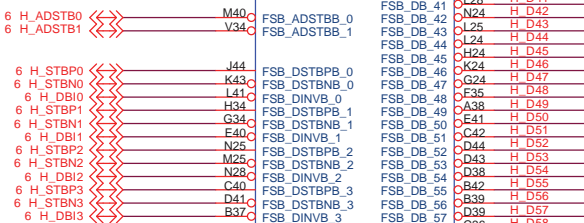
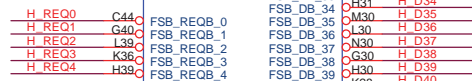
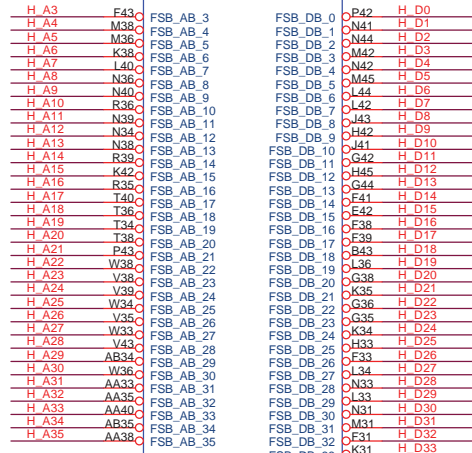
8 H_REQ[0..4] <<> H_REQ[0..4]
8 H_A[3..35] <<> H_A[3..35]
8 H_D[0..63] <<> H_D[0..63]



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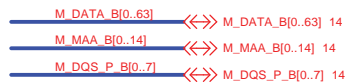


abit
UNIVERSAL ABIT

MCH Part1 FSB & PCIE X16

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13,14 DDR3_DRAMRST <<

DDR E

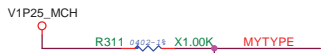


BSEL TABLE			
2	1	0	PSB FREQUENCY
0	0	1	133 MHZ (533)
0	1	0	200 MHZ (800)
0	0	0	267 MHZ (1067)

EXP_SLR : PCI-EXPRESS LANE REVERSAL

H NORM

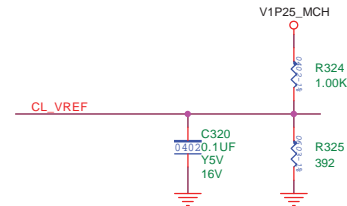
L REVERSE



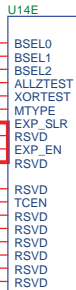
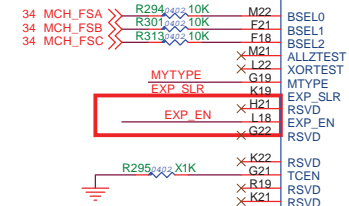
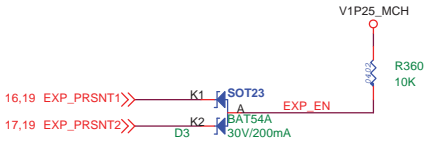
MYTYPE : MEMORY TYPE

H DDR2 TYPE R311

L DDR3 TYPE R306



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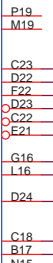
MISC



NC



X38



VCC3_3

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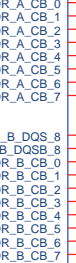
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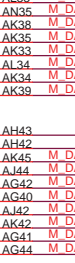
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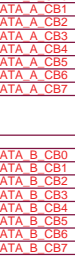
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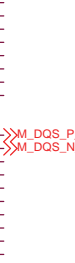
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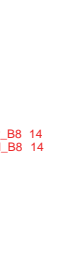
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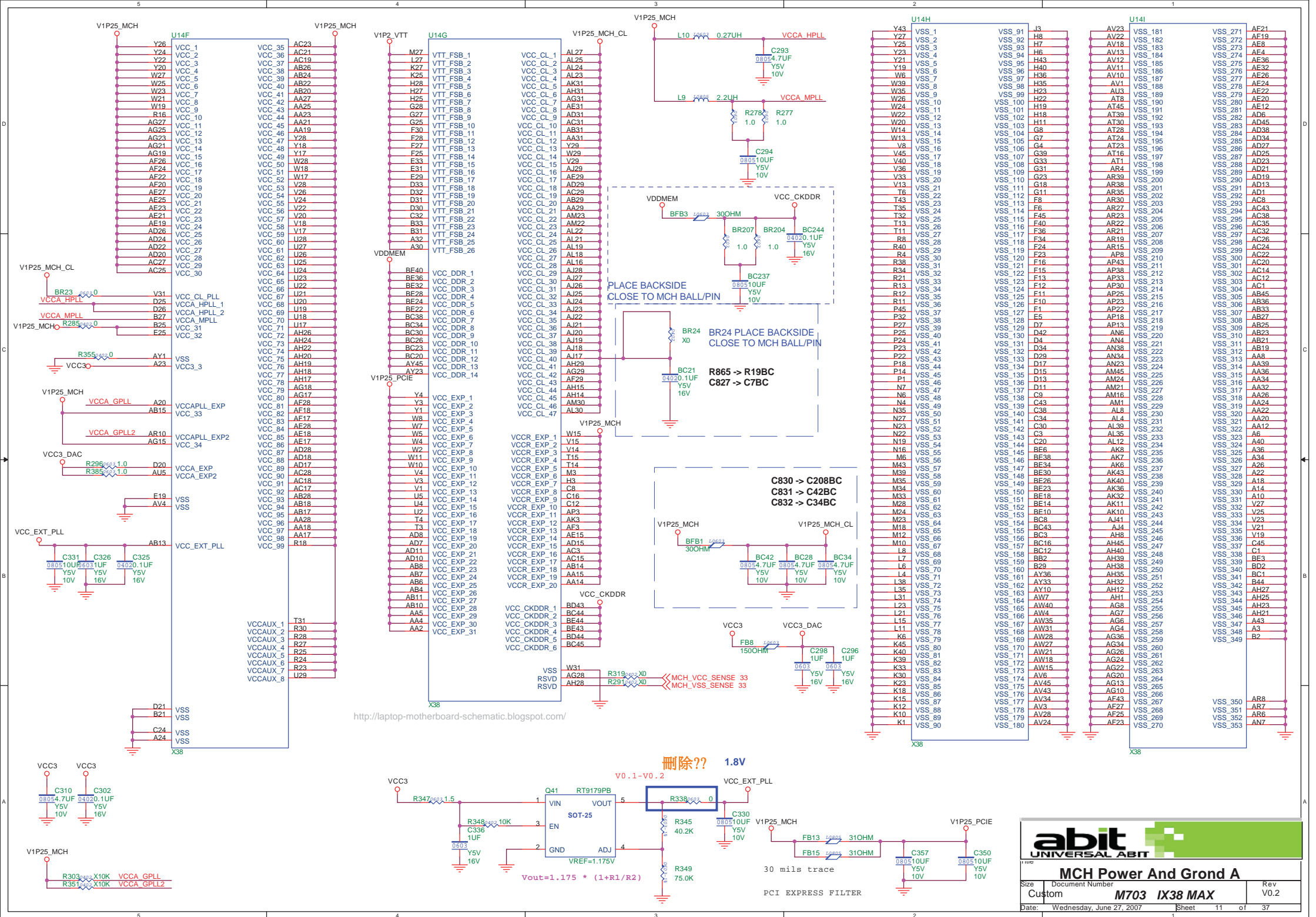
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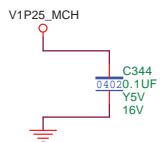
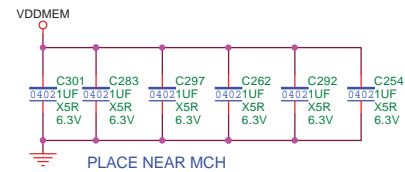
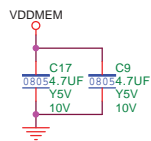
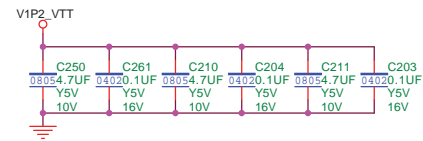
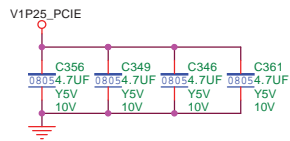
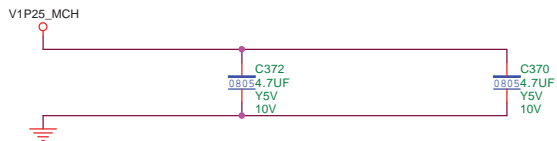
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VSS

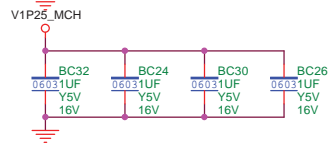
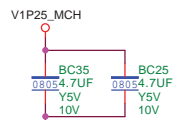
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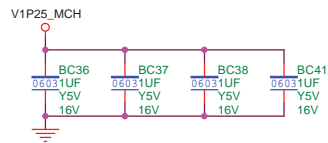




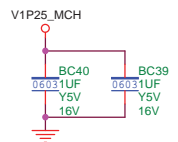
PLACE BACKSIDE



C858 -> C1BC
C860 -> C2BC
C862 -> C3BC
C864 -> C4BC



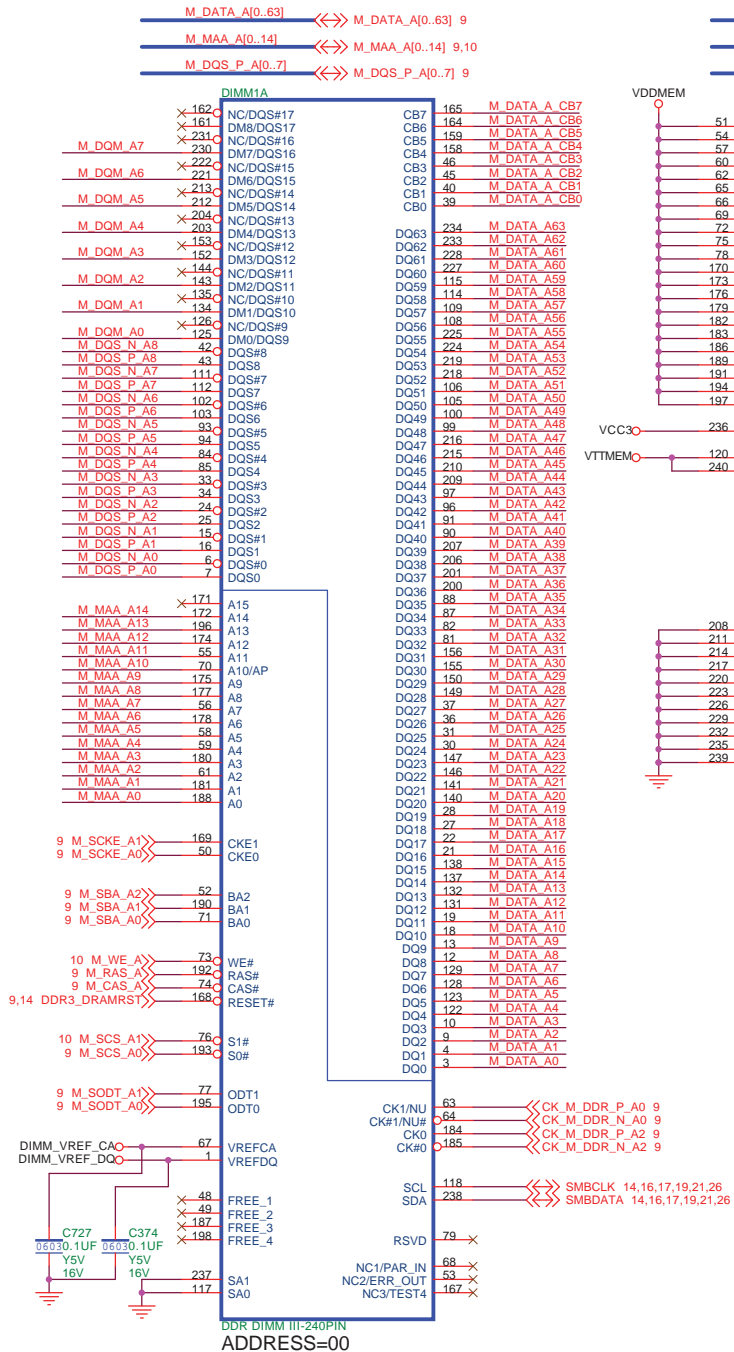
C872 -> C8BC
C874 -> C9BC
C876 -> C11BC
C878 -> C13BC



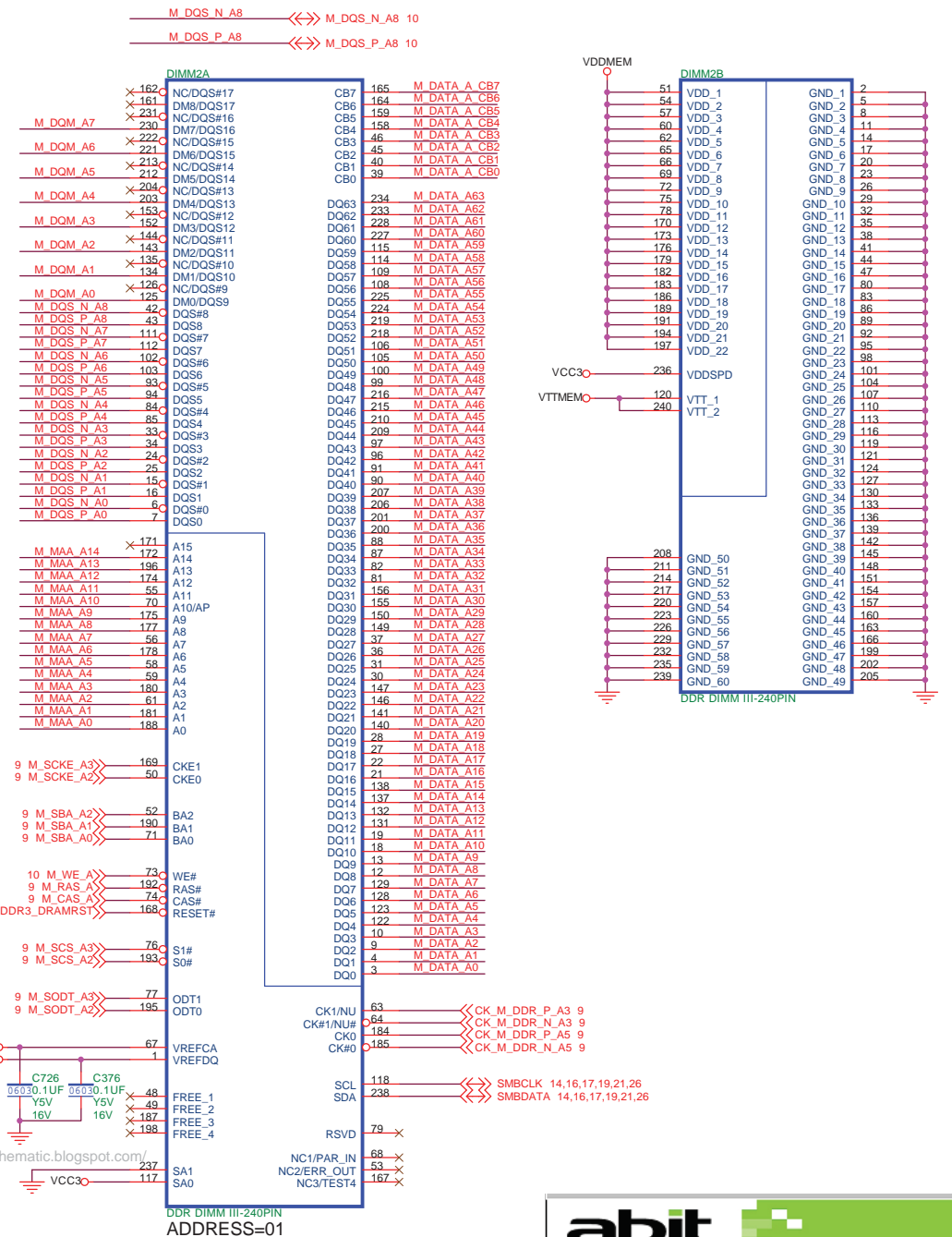
C880 -> C17BC
C882 -> C19BC

<http://laptop-motherboard-schematic.blogspot.com/>

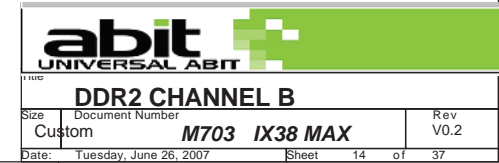
DDR III Channel A DIMM1

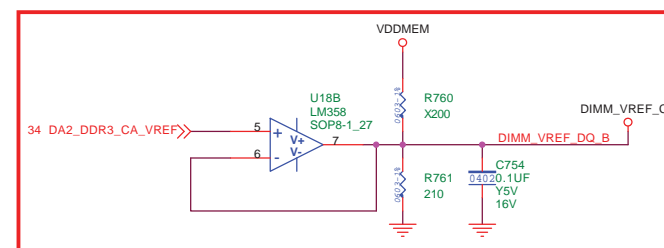
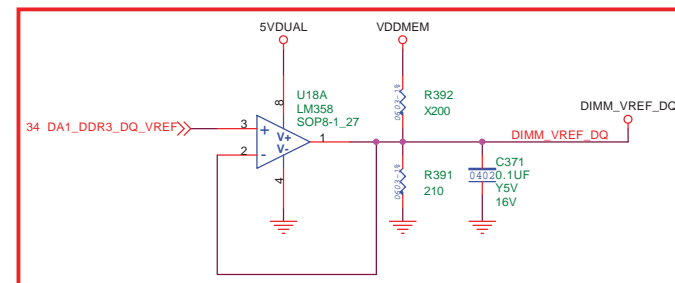
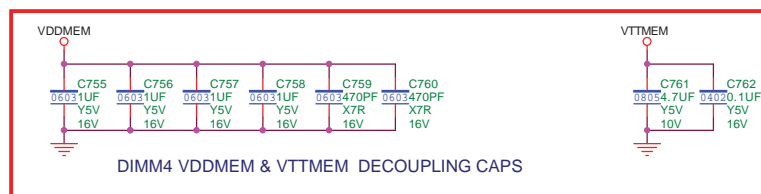
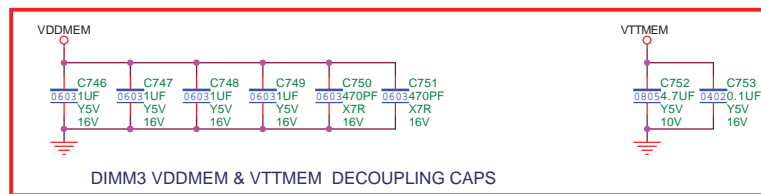
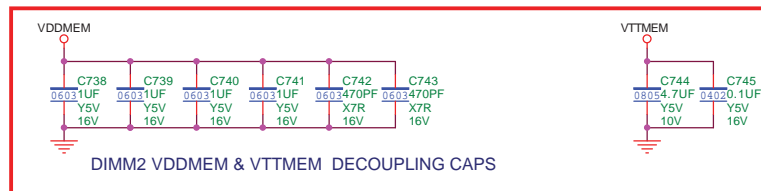
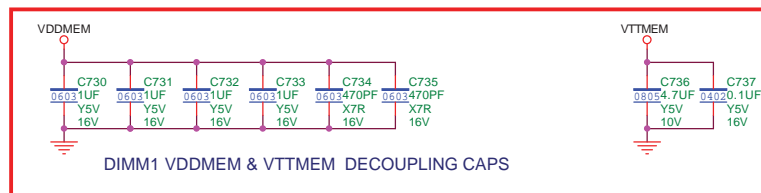


DDR III Channel A DIMM2

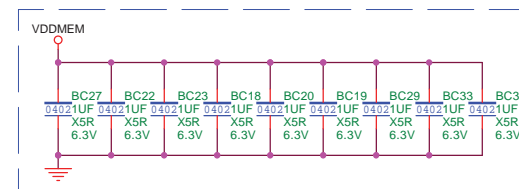



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DDR III Channel B DIMM2
```

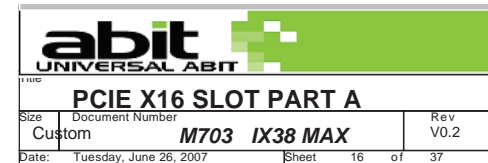




PLACE BACKSIDE



<http://laptop-motherboard-schematic.blogspot.com/>



<<GEXP_RXN_B[15..0] 8
>>GEXP_RXP_B[15..0] 8
<<GEXP_TXN_B[15..0] 8
>>GEXP_TXP_B[15..0] 8

8 GEXP_TXP_B0>> C554 0.1UF GEXP_TXP_C_B0
Y5V 16V
8 GEXP_TXN_B0>> C553 0.1UF GEXP_TXN_C_B0
Y5V 16V

8 GEXP_TXP_B1>> C559 0.1UF GEXP_TXP_C_B1
Y5V 16V
8 GEXP_TXN_B1>> C558 0.1UF GEXP_TXN_C_B1
Y5V 16V

8 GEXP_TXP_B2>> C561 0.1UF GEXP_TXP_C_B2
Y5V 16V
8 GEXP_TXN_B2>> C560 0.1UF GEXP_TXN_C_B2
Y5V 16V

8 GEXP_TXP_B3>> C563 0.1UF GEXP_TXP_C_B3
Y5V 16V
8 GEXP_TXN_B3>> C562 0.1UF GEXP_TXN_C_B3
Y5V 16V

8 GEXP_TXP_B4>> C565 0.1UF GEXP_TXP_C_B4
Y5V 16V
8 GEXP_TXN_B4>> C564 0.1UF GEXP_TXN_C_B4
Y5V 16V

8 GEXP_TXP_B5>> C567 0.1UF GEXP_TXP_C_B5
Y5V 16V
8 GEXP_TXN_B5>> C566 0.1UF GEXP_TXN_C_B5
Y5V 16V

8 GEXP_TXP_B6>> C569 0.1UF GEXP_TXP_C_B6
Y5V 16V
8 GEXP_TXN_B6>> C568 0.1UF GEXP_TXN_C_B6
Y5V 16V

8 GEXP_TXP_B7>> C571 0.1UF GEXP_TXP_C_B7
Y5V 16V
8 GEXP_TXN_B7>> C570 0.1UF GEXP_TXN_C_B7
Y5V 16V

8 GEXP_TXP_B8>> C573 0.1UF GEXP_TXP_C_B8
Y5V 16V
8 GEXP_TXN_B8>> C572 0.1UF GEXP_TXN_C_B8
Y5V 16V

8 GEXP_TXP_B9>> C575 0.1UF GEXP_TXP_C_B9
Y5V 16V
8 GEXP_TXN_B9>> C574 0.1UF GEXP_TXN_C_B9
Y5V 16V

8 GEXP_TXP_B10>> C577 0.1UF GEXP_TXP_C_B10
Y5V 16V
8 GEXP_TXN_B10>> C576 0.1UF GEXP_TXN_C_B10
Y5V 16V

8 GEXP_TXP_B11>> C579 0.1UF GEXP_TXP_C_B11
Y5V 16V
8 GEXP_TXN_B11>> C578 0.1UF GEXP_TXN_C_B11
Y5V 16V

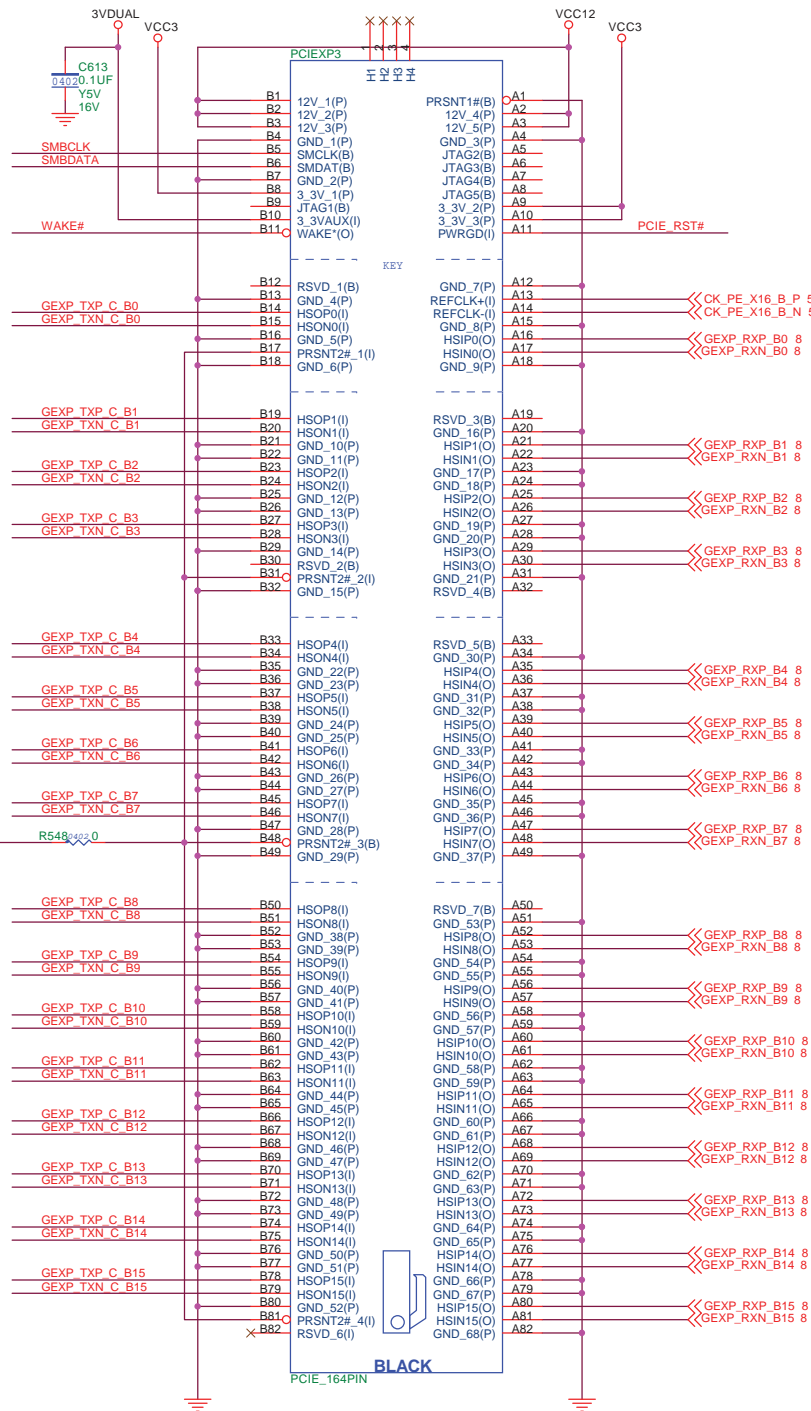
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Y5V 16V
8 GEXP_TXN_B12>> C580 0.1UF GEXP_TXN_C_B12
Y5V 16V

8 GEXP_TXP_B13>> C583 0.1UF GEXP_TXP_C_B13
Y5V 16V
8 GEXP_TXN_B13>> C582 0.1UF GEXP_TXN_C_B13
Y5V 16V

8 GEXP_TXP_B14>> C585 0.1UF GEXP_TXP_C_B14
Y5V 16V
8 GEXP_TXN_B14>> C584 0.1UF GEXP_TXN_C_B14
Y5V 16V

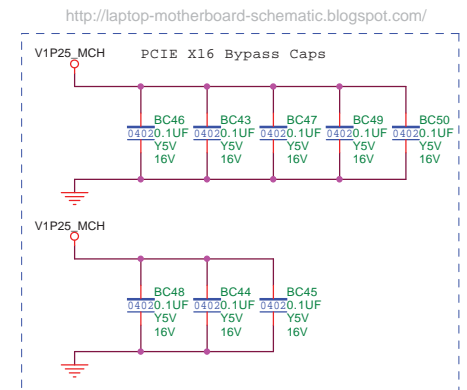
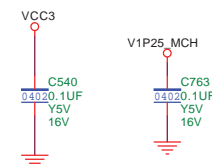
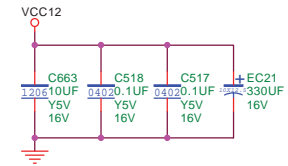
8 GEXP_TXP_B15>> C587 0.1UF GEXP_TXP_C_B15
Y5V 16V
8 GEXP_TXN_B15>> C586 0.1UF GEXP_TXN_C_B15
Y5V 16V

10,19 EXP_PRSNT2<< R548<<0

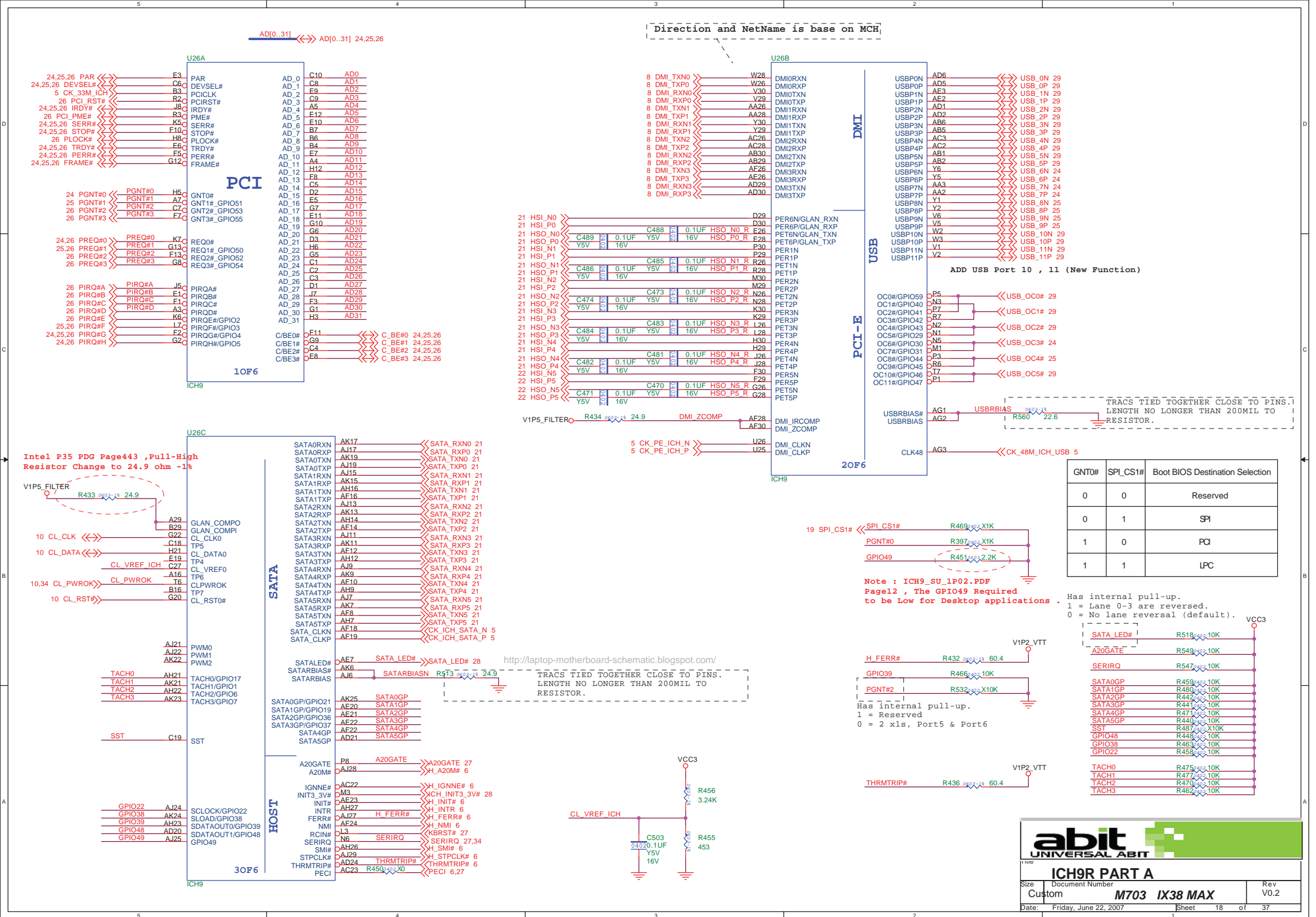


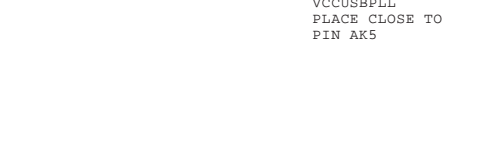
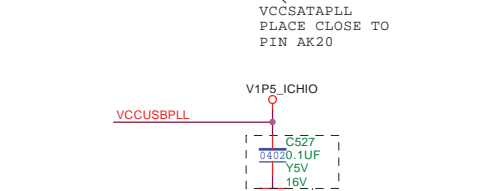
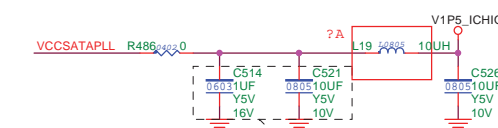
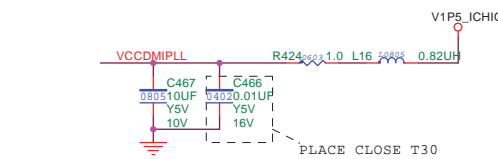
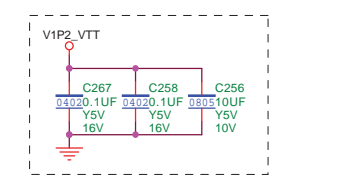
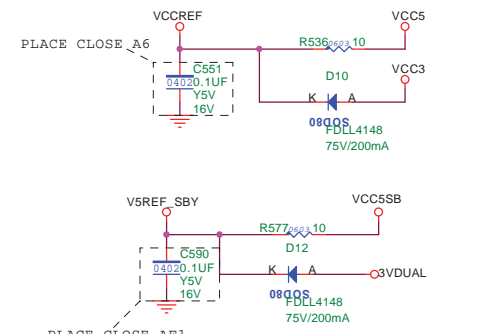
PCIE_RST# << PCIE_RST# 16,21,27
WAKE# >> WAKE# 16,19,21

SMBDATA <<< SMBDATA 13,14,16,19,21,26
SMBCLK <<< SMBCLK 13,14,16,19,21,26



Place at BACK SIDE near MCH pin





DD3_R RN8-11 8 33 DD3
DD12_R RN8-22 7 33 DD12
DD2_R RN8-33 6 33 DD2
DD13_R RN8-44 5 33 DD13

DD5_R RN6-11 8 33 DD5
DD10_R RN6-22 7 33 DD10
DD4_R RN6-33 6 33 DD4
DD11_R RN6-44 5 33 DD11

DD7_R RN5-11 8 33 DD7
DD8_R RN5-22 7 33 DD8
DD6_R RN5-33 6 33 DD6
DD9_R RN5-44 5 33 DD9

DD1_R RN7-11 8 33 DD1
DD14_R RN7-22 7 33 DD14
DD0_R RN7-33 6 33 DD0
DD15_R RN7-44 5 33 DD15

DA1_R RN4-11 8 33 DA1
DA0_R RN4-22 7 33 DA0
DA2_R RN4-33 6 33 DA2
DCS0#_R RN4-44 5 33 DCS0#

DCS1#_R R199 33 DCS1#

DDACK#_R R249 22 DDACK#

DDREQ#_R R271 82 DDREQ

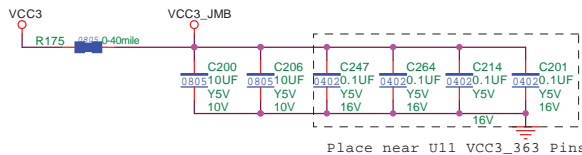
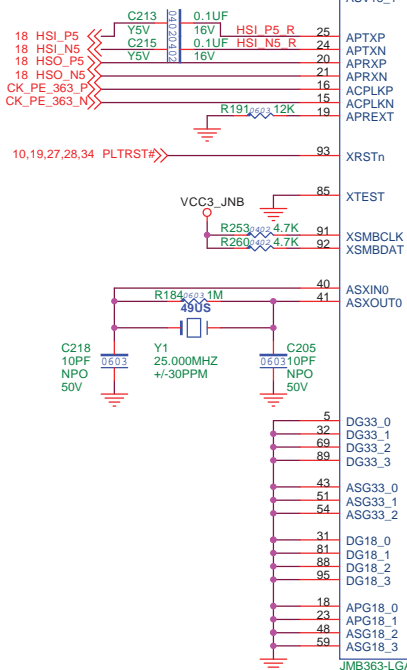
DIOR#_R R251 22 DIOR#

DIOW#_R R252 22 DIOW#

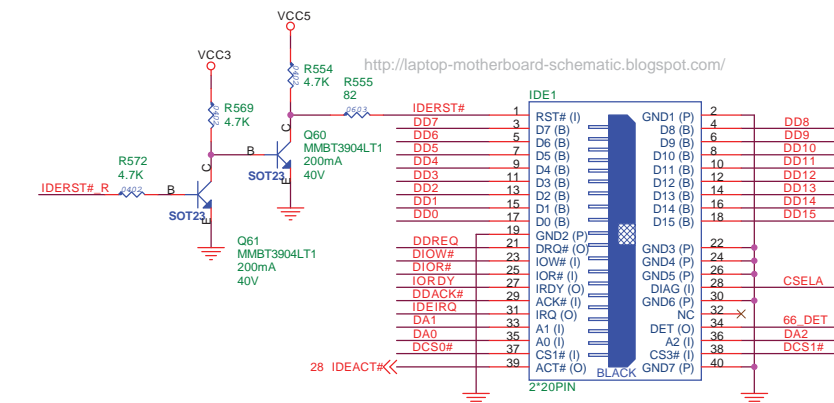
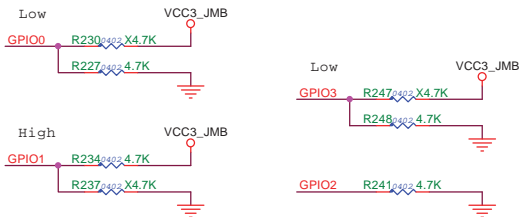
IORDY#_R R250 82 IORDY#

IDEIRQ#_R R215 82 IDEIRQ#

V0.1-V0.2



Place near U11 VCC3_363 Pins



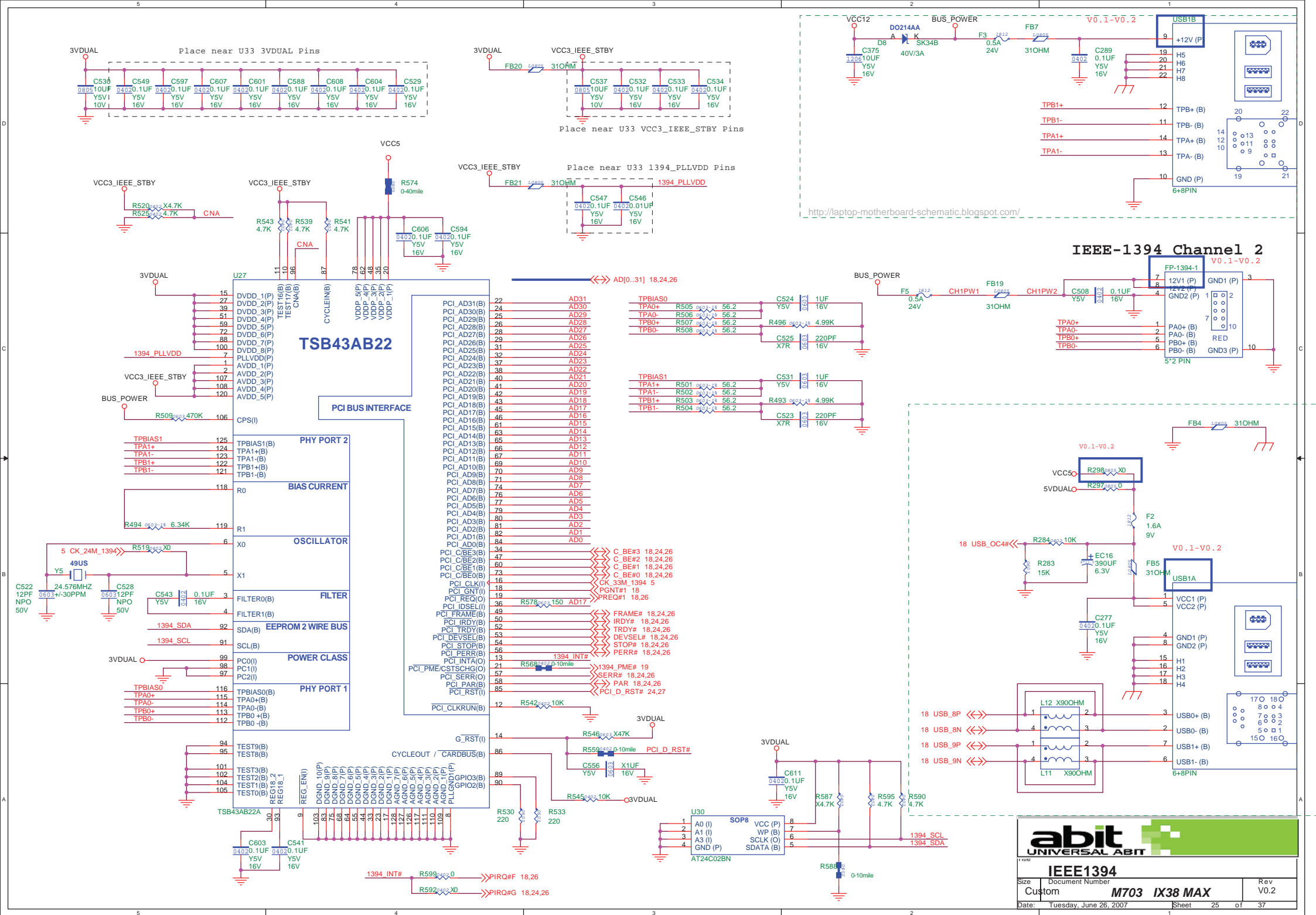
abit
UNIVERSAL ABIT

PCI EXPRESS PATA CONTROLLER

Size: Document Number: M703 IX38 MAX Rev: V0.2

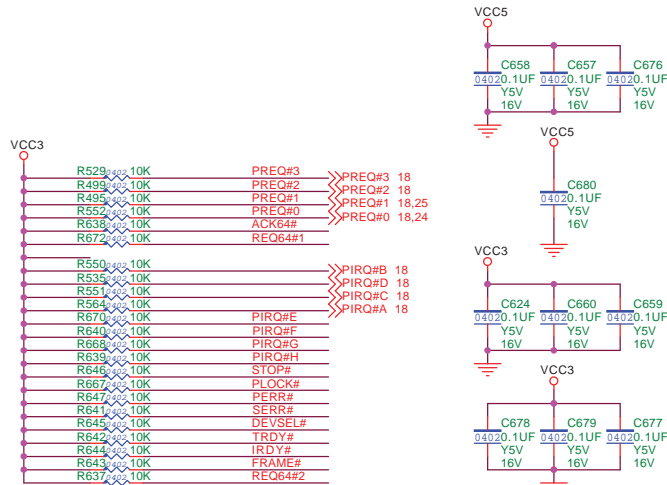
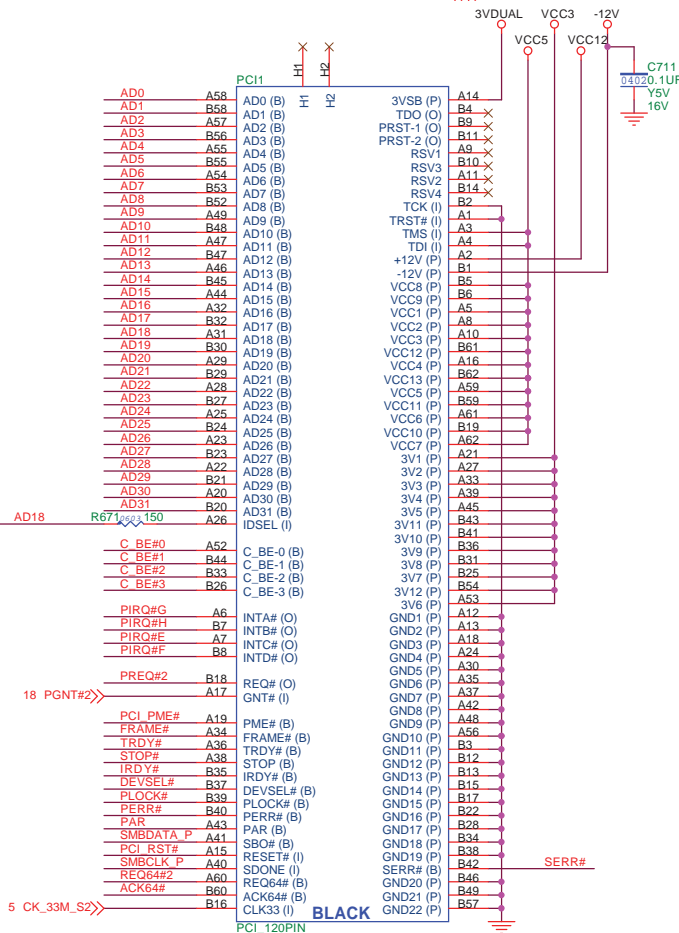
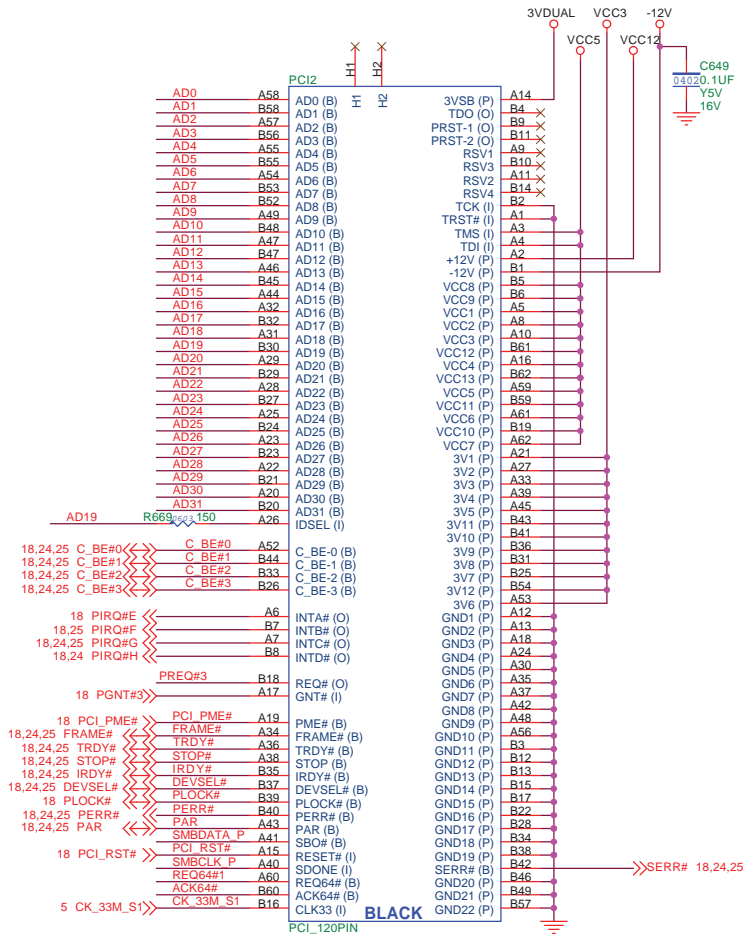
Custom

Date: Friday, June 22, 2007 Sheet 22 of 37

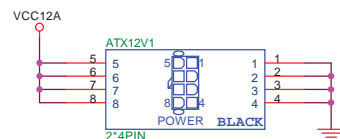
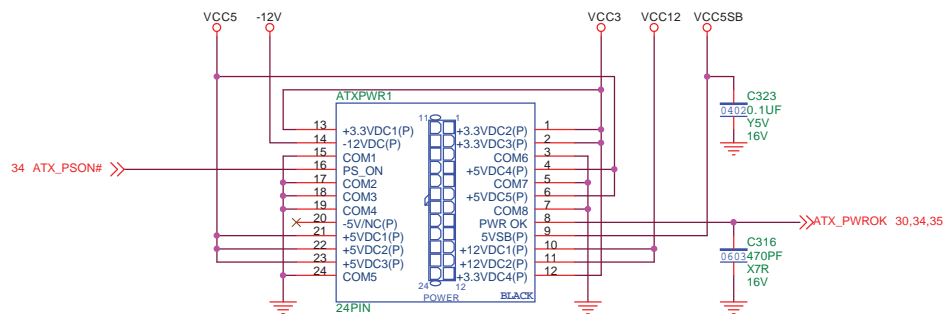


18,24,25 AD[0..31] <<>

5,30,34 AC05_SCL <<>
5,30,34 AC05_SDA <<>
R333 X0
R330 X0
R601 X0
R602 X0
SMBCLK P
SMBDATA P
SMBCLK 13,14,16,17,19,21
SMBDATA 13,14,16,17,19,21



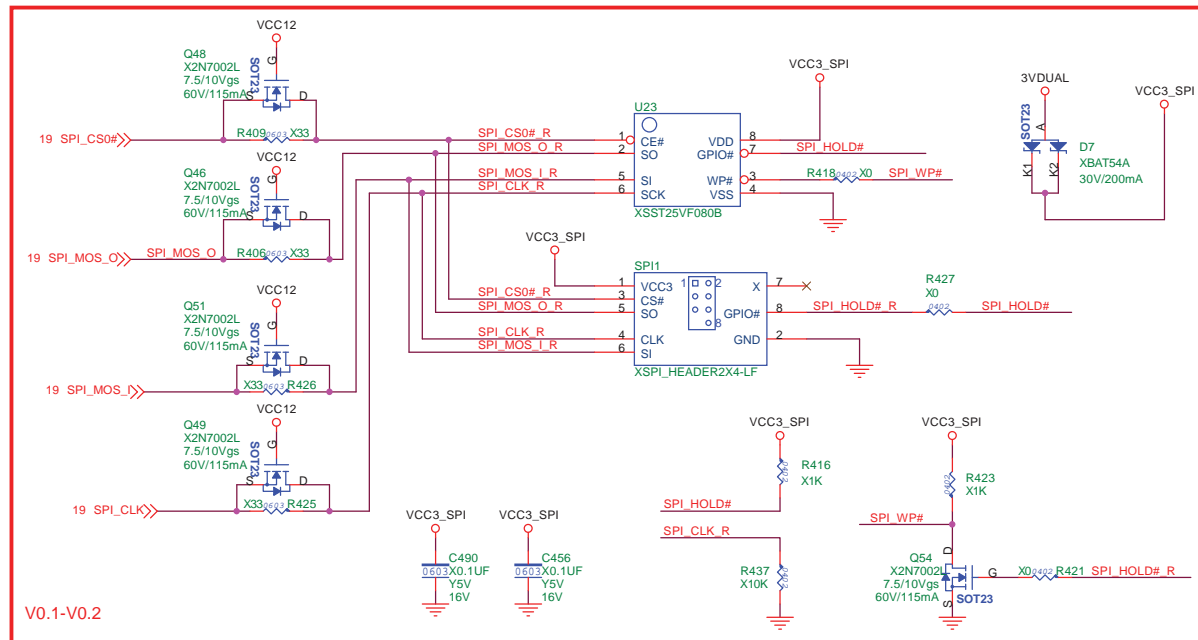
<http://laptop-motherboard-schematic.blogspot.com/>



POWER CONNECTOR DECOUPLING

V0.1-V0.2

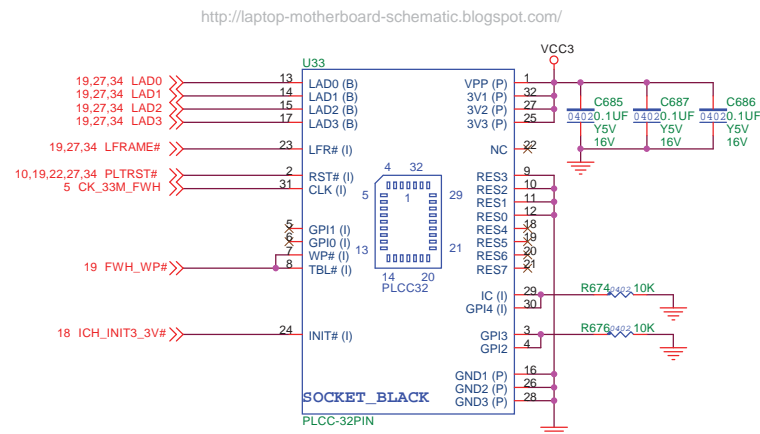
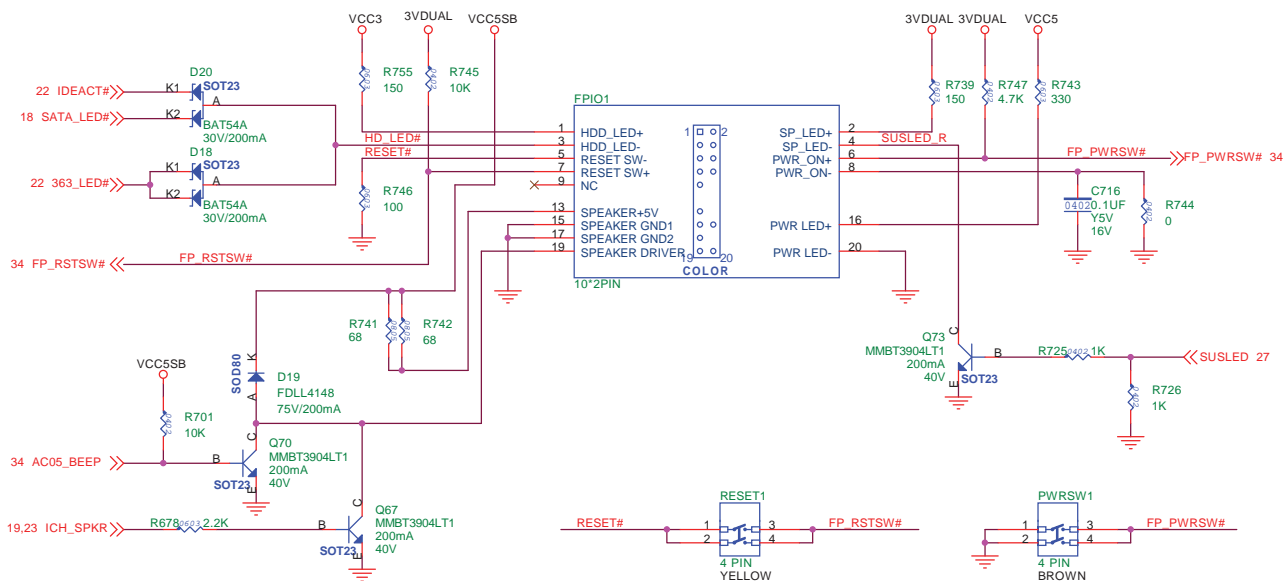
Del ATX4P1



V0.1-V0.2

V0.1-V0.2

Del SMB1

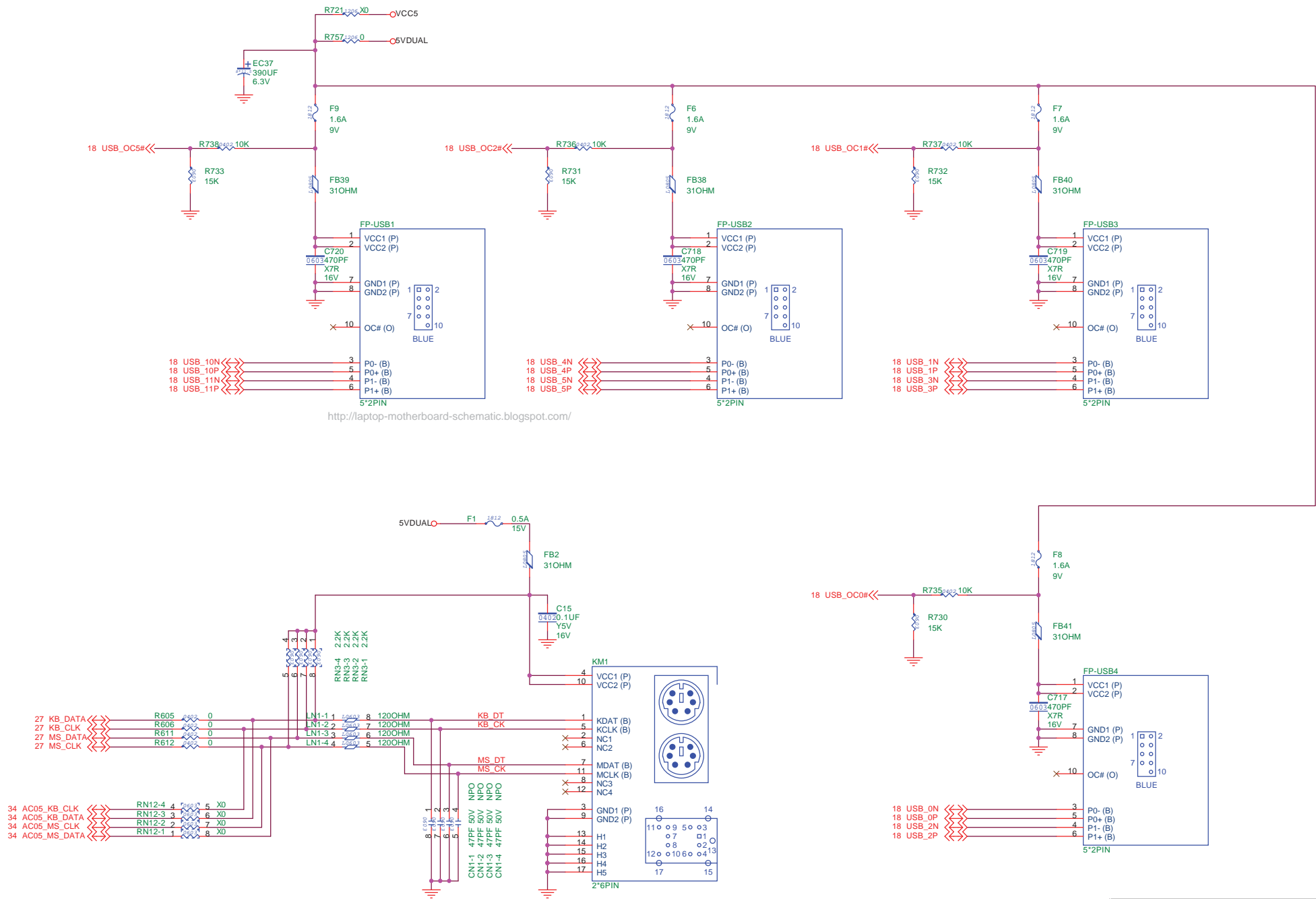


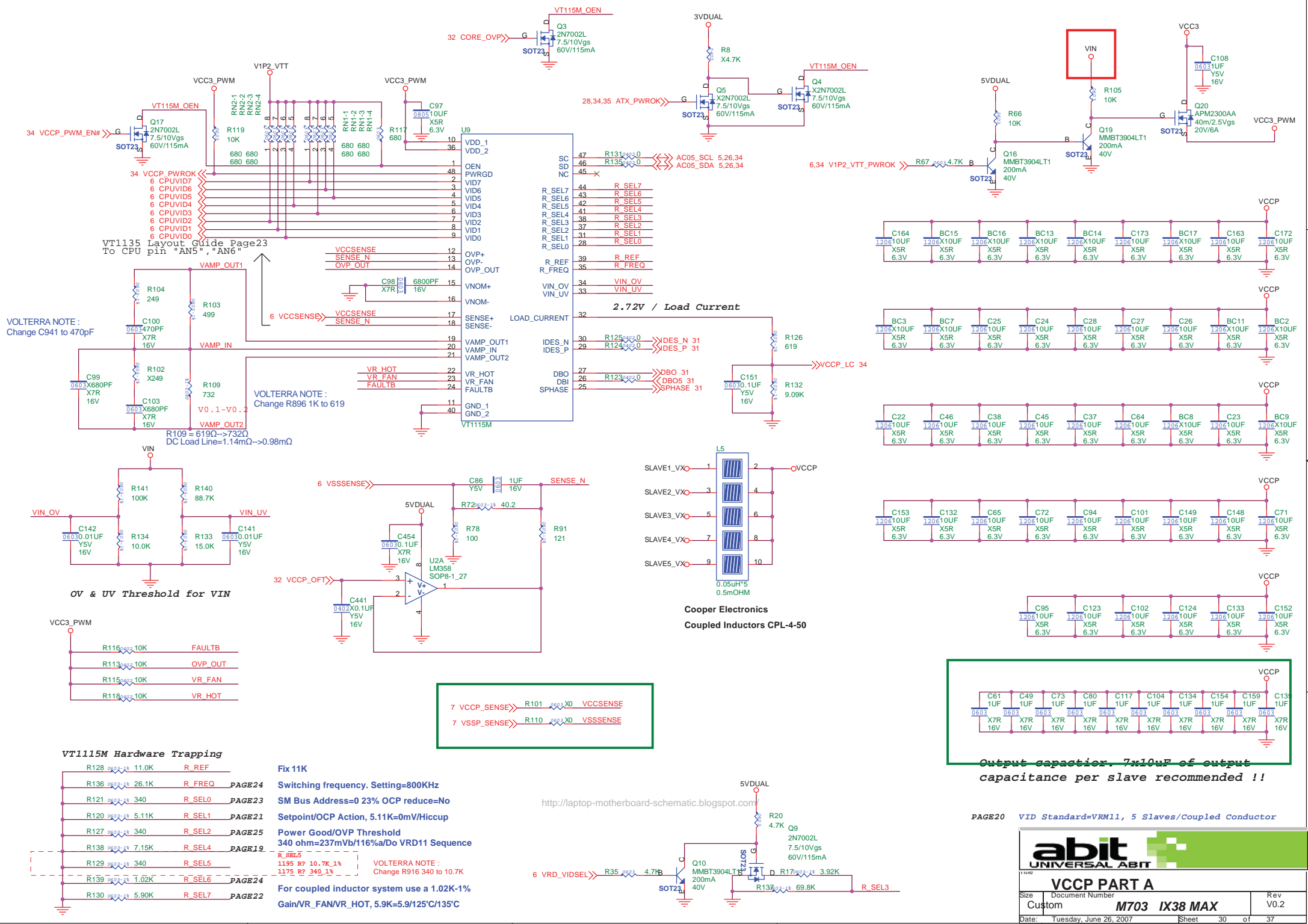
abit
UNIVERSAL ABIT

FPIO, FW, SMB & ATX

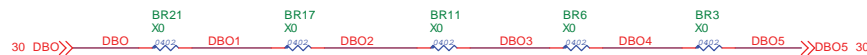
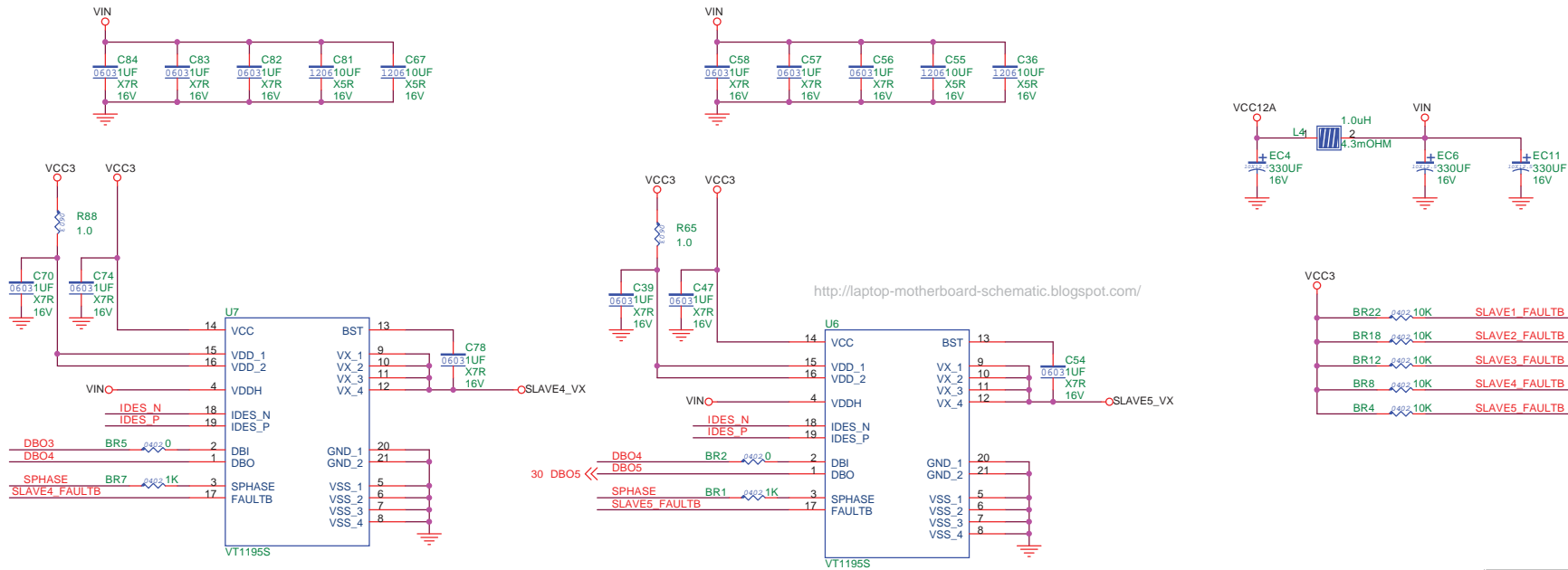
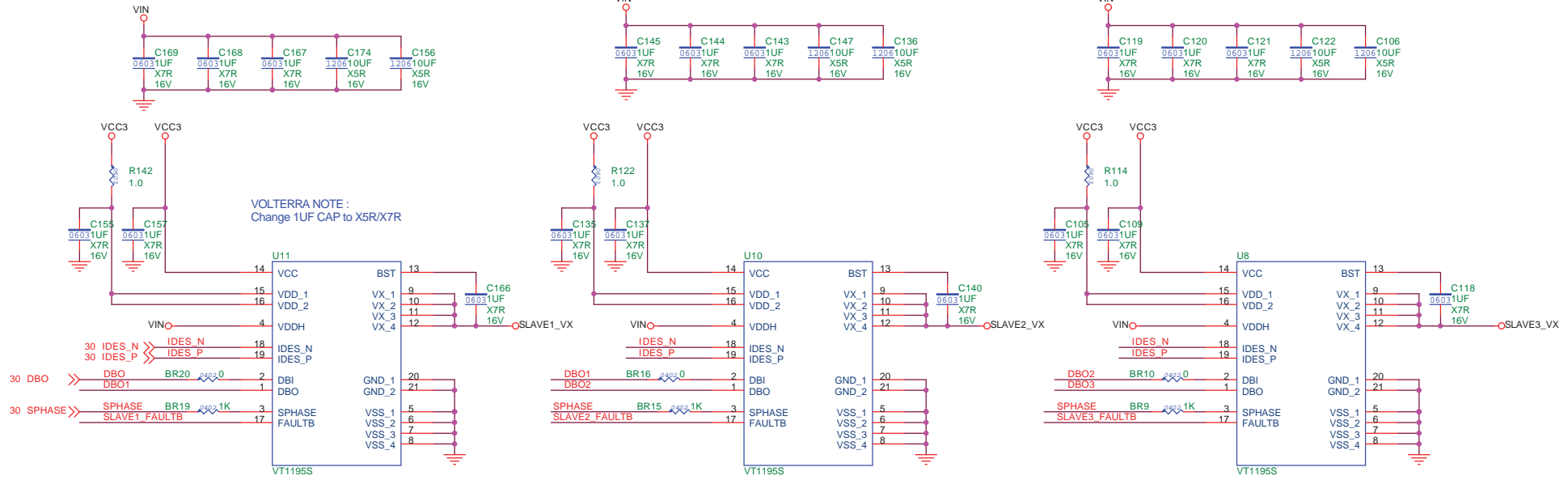
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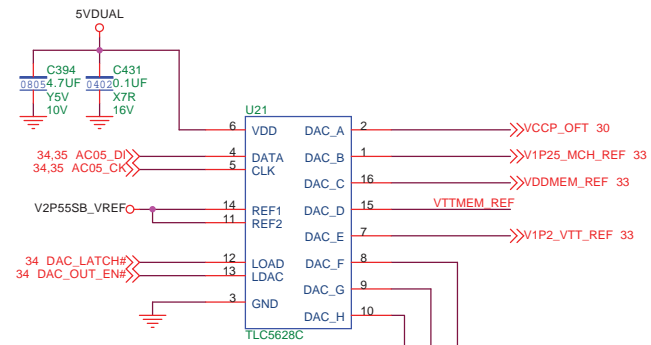
Date: Friday, June 22, 2007 Sheet 28 of 37



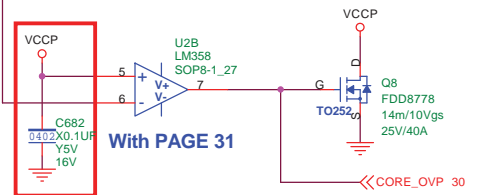
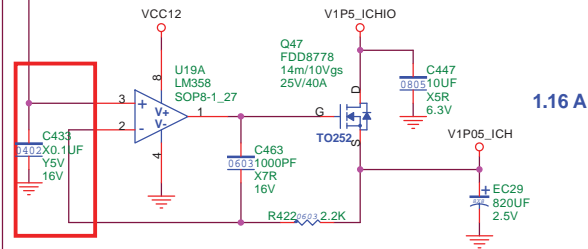
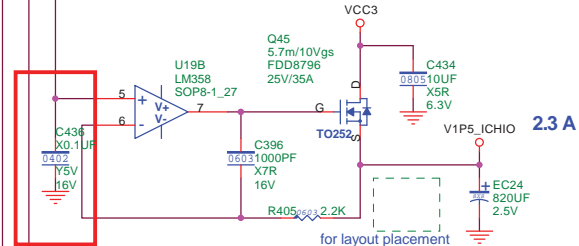
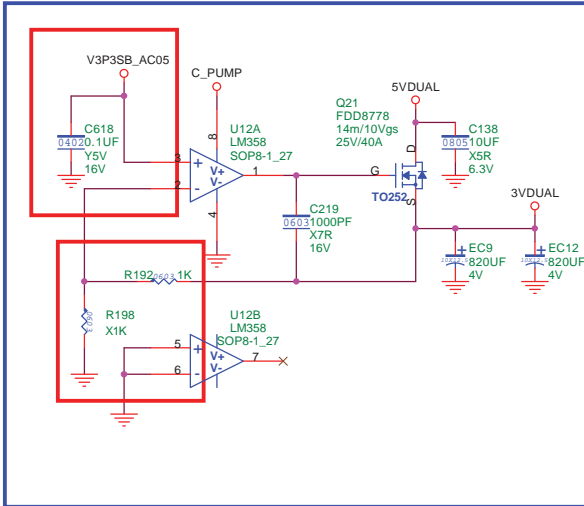


input capacitor. 3x1uF and 2x10uF
of input capacitance per slave recommended !!

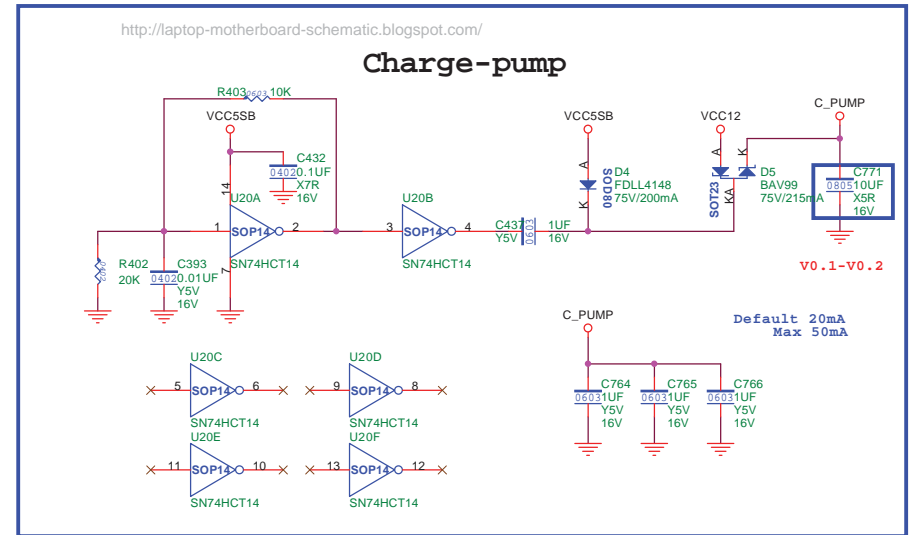
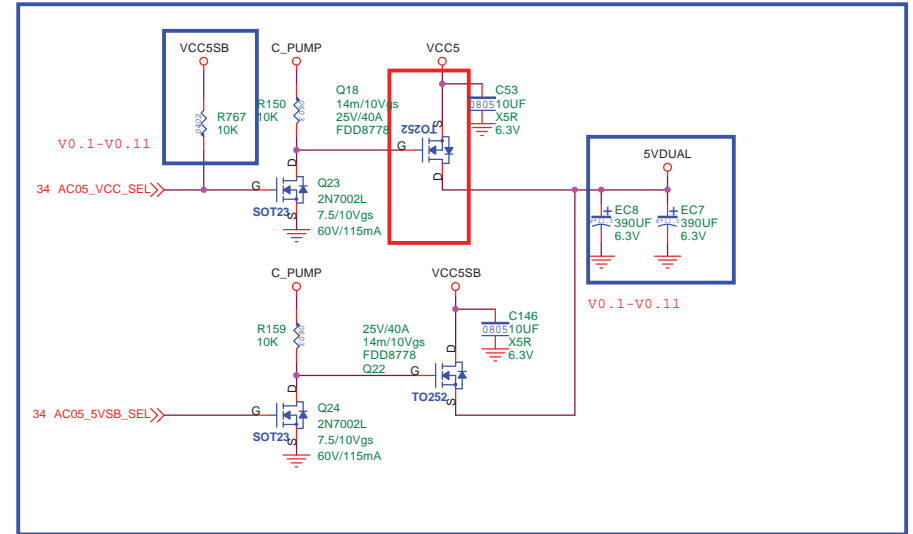
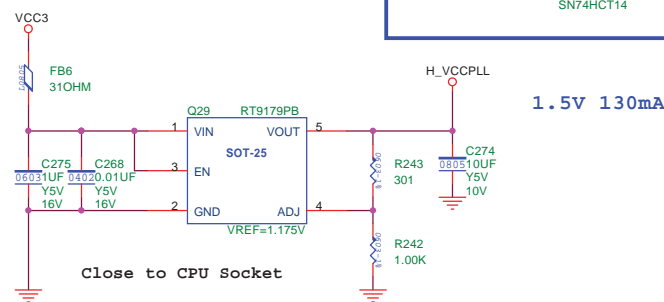
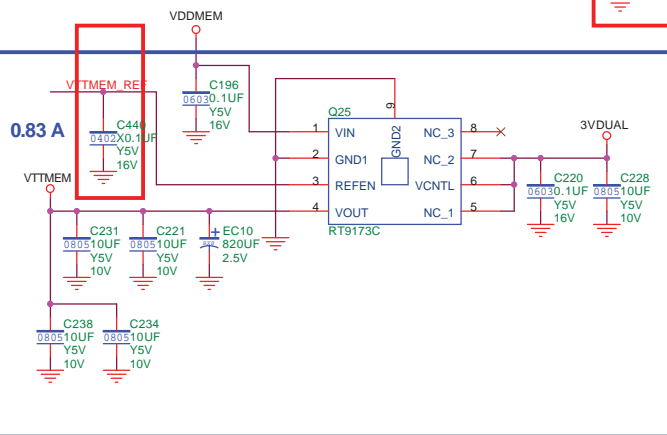


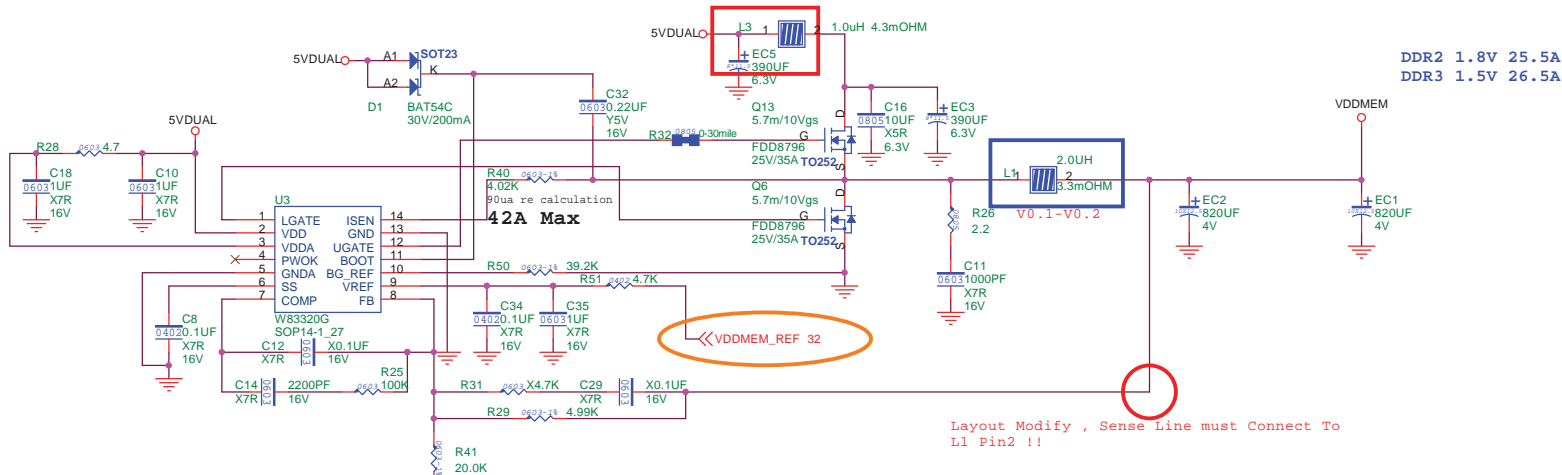
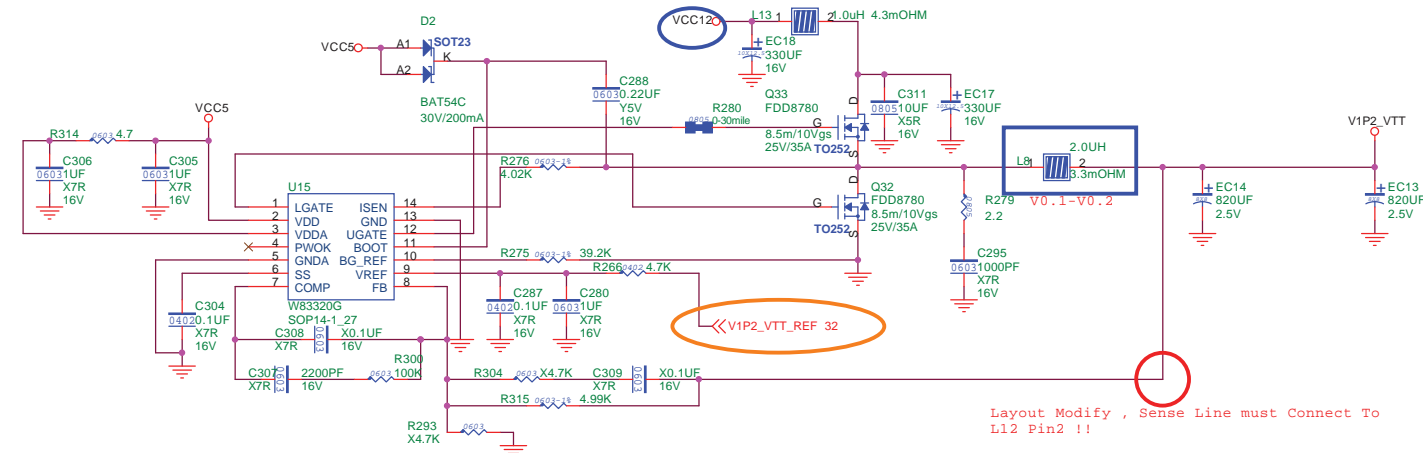
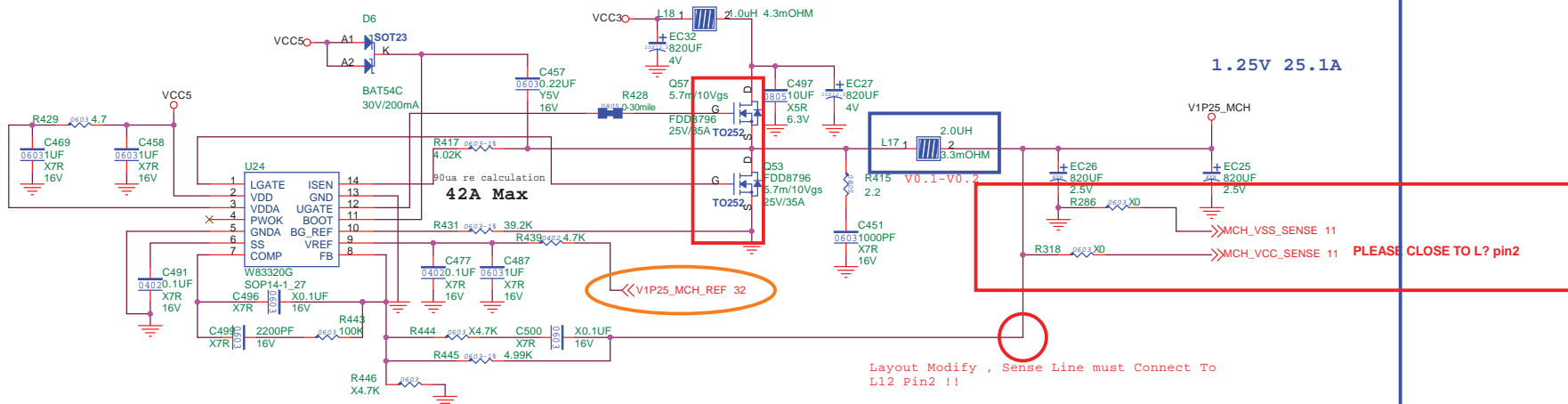


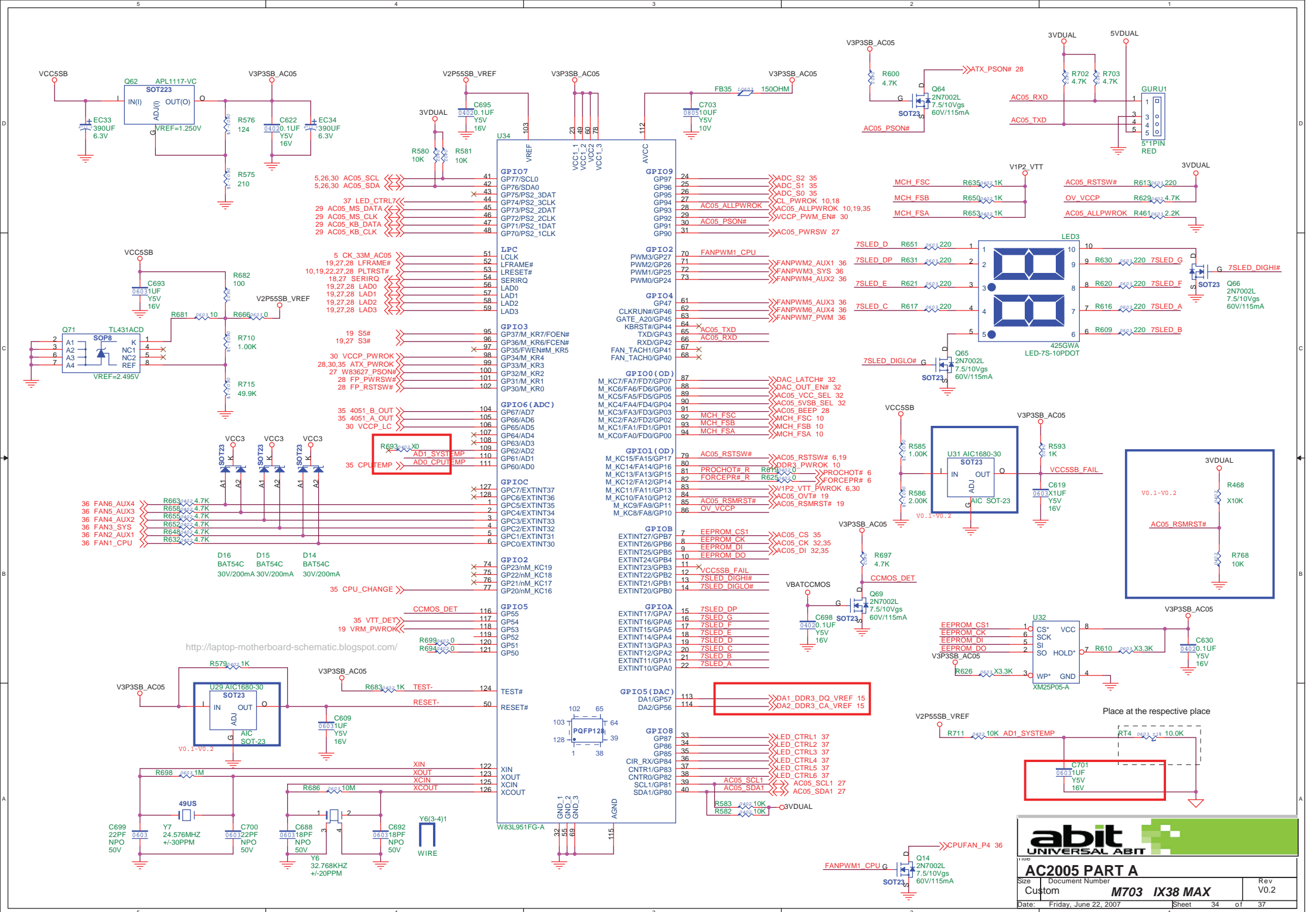
3.3V

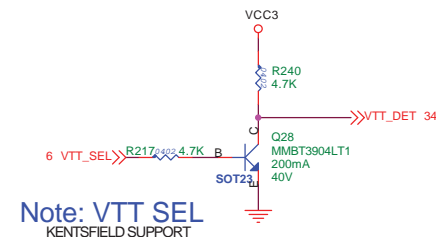
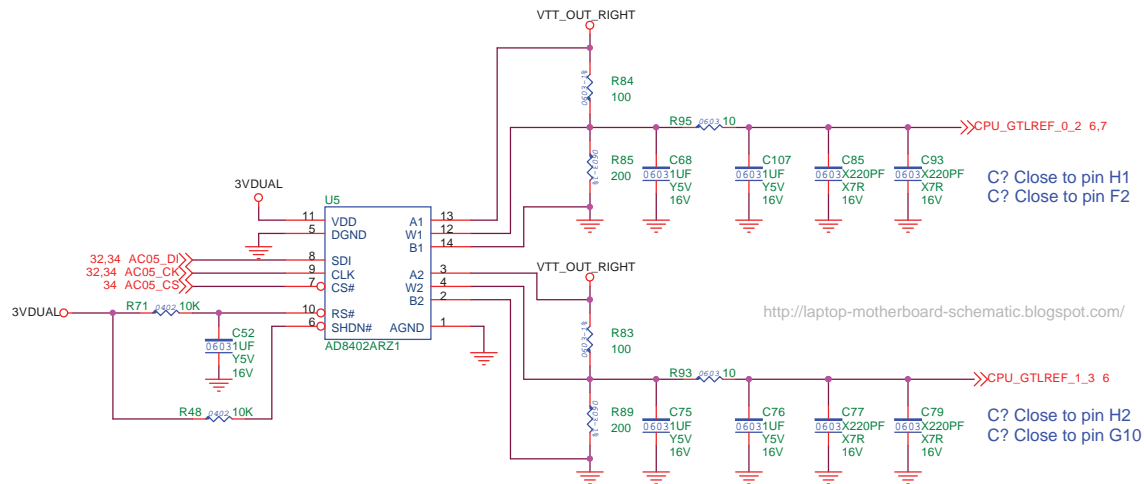
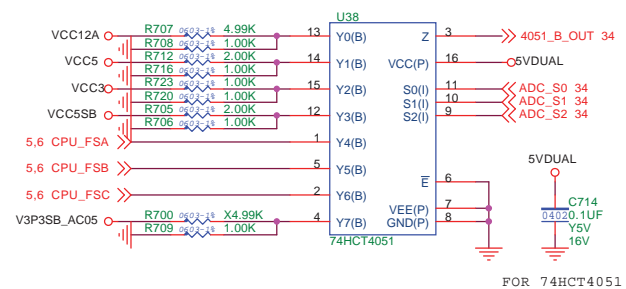
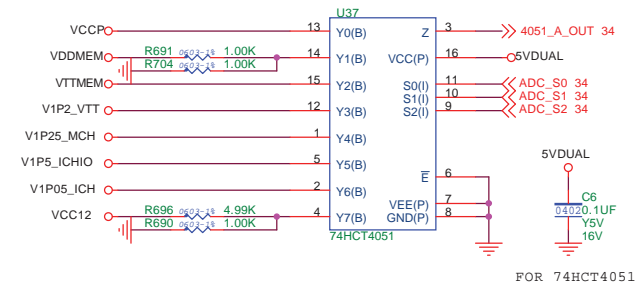
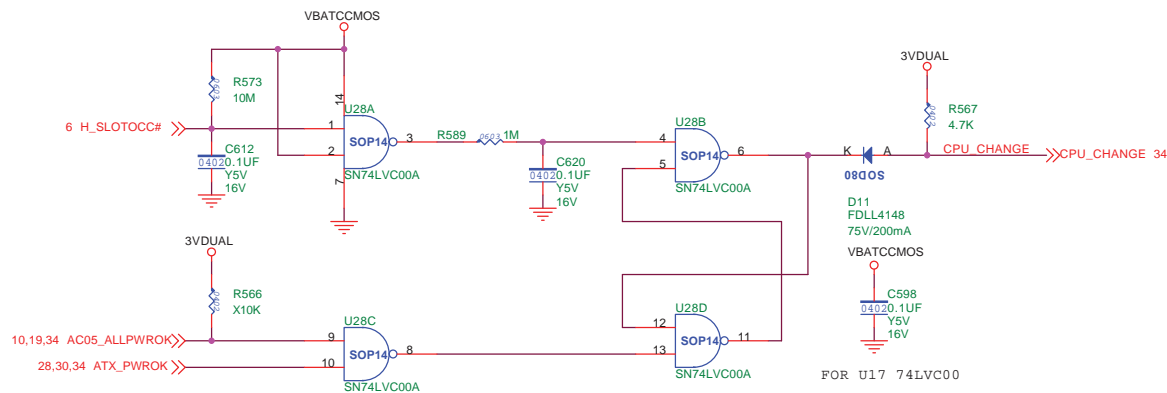
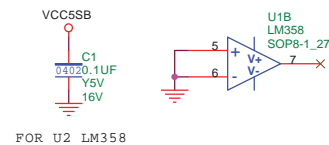
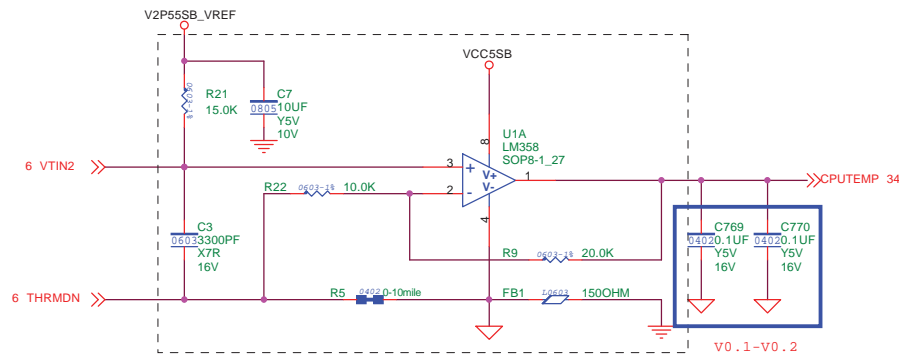


Note: VCCP OVT



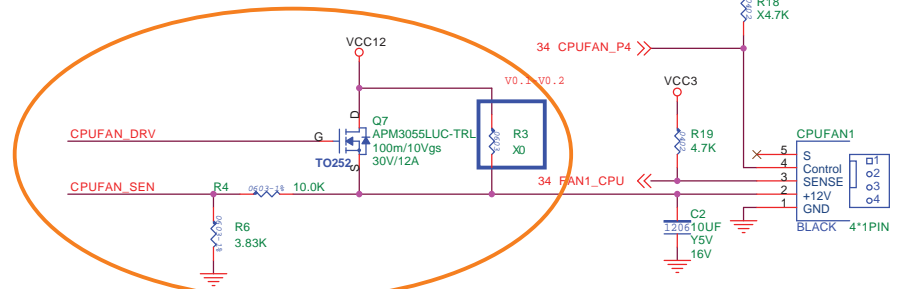
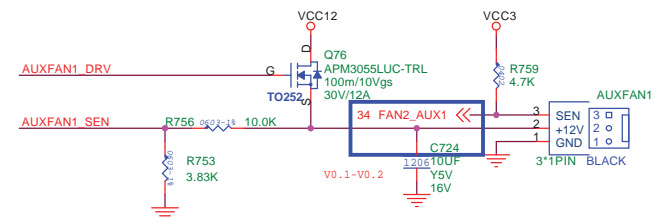
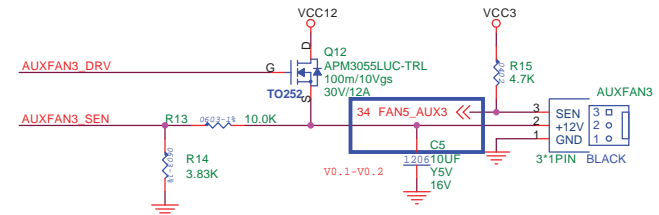
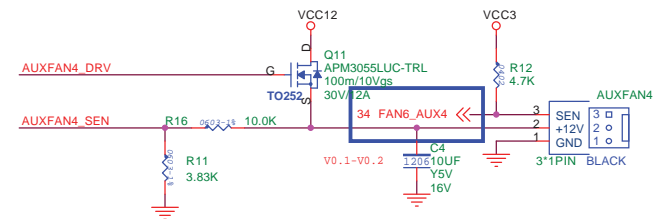
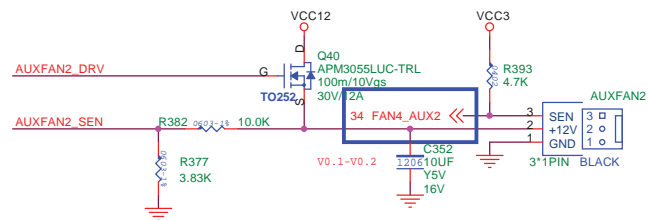
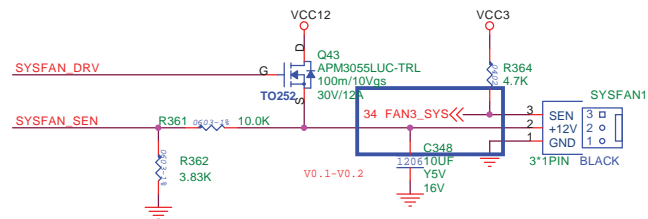
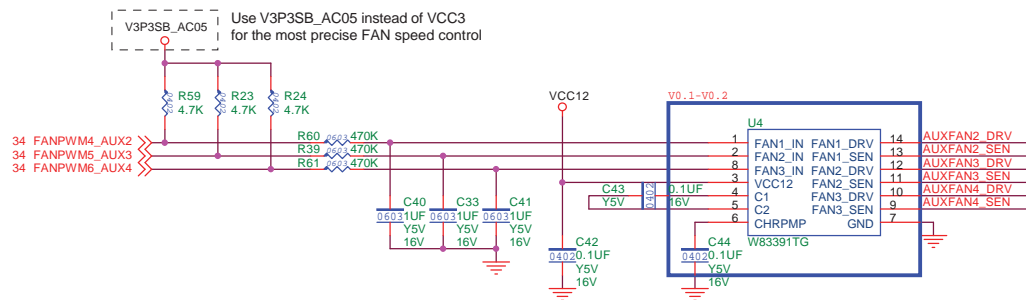
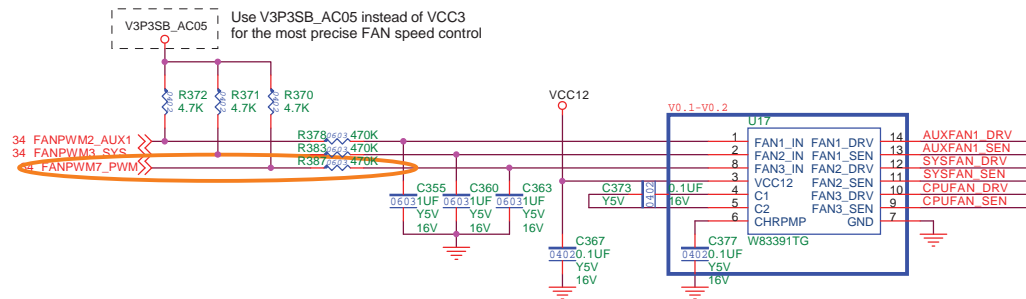






Note: VTT_SEL
KENTSFIELD SUPPORT

If CPU VTT_SEL used,
- VTT_SEL= 1, VTT= 1.2V
- VTT_SEL= 0, VTT= 1.1V



New Circuit Support 3*1Pin FAN Control

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